

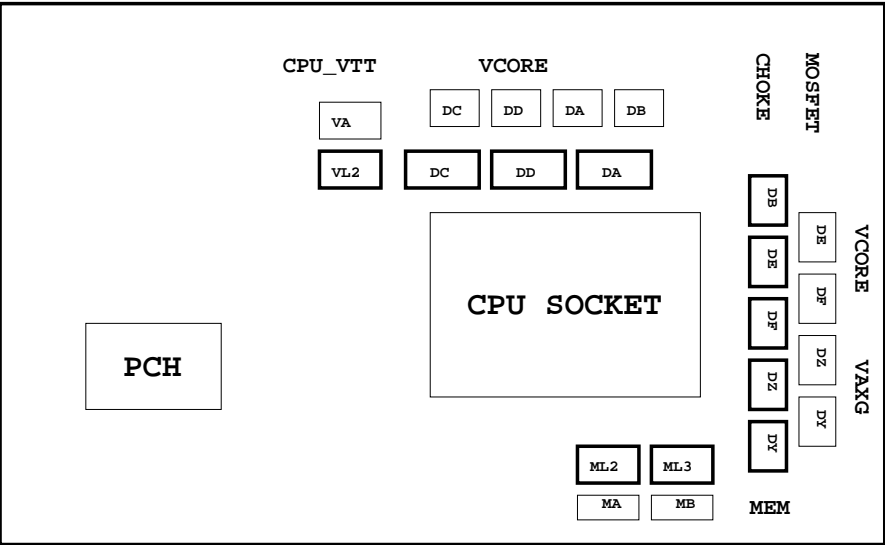
Model Name: GA-Z77X-UD3H-WB 1.1

SHEET TITLE

01	COVER SHEET
02	BOM & PCB MODIFY HISTORY
03	BLOCK DIAGRAM
04	CPU_LGA1155-A
05	CPU_LGA1155-B
06	CPU_LGA1155-C
07	DDR III CHANNEL A
08	DDR III CHANNEL B
09	PCH_FDI,DMI,USB,PCIE
10	PCH_DP_HDMI_DVI_DAC,CLK BUFFER
11	PCH_HOST,SATA,PCI
12	PCH_GPIO,CTRL,AUDIO
13	PCH_PWR,GND
14	PCI EXPRESS*16 SLOT
15	PCI EXPRESS*8 SLOT
16	PCI EXPRESS*16/*8 SWITCH
17	PCI EXPRESS*1 SLOTS X3
18	PCI EXPRESS*4 SLOT / SWITCH
19	IT8892 PCIE to PCI BRIDGE
20	PCI SLOT
21	DP / HDMI / DVI Connector
22	mSATA Connector
23	Dual BIOS , TPM
24	VT2021
25	REAR AUDIO JACK
26	VCORE PWM_IR3567-1
27	VCORE PWM_IR3567-2

SHEET TITLE

28	DDR_15V & CPUVTT PWM_IR3570-1
29	DDR_15V & CPUVTT PWM_IR3570-2
30	DISCRETE POWER 1
31	DISCRETE POWER 2
32	I/O IT8728F
33	USB3_ESATA , KB/USB3, -PHOT
34	F_PANEL , F_USB , F_USB3
35	ATX POWER, CLOCK GEN
36	HWM, FAN CTRL
37	Atheros 8151
38	ESATA SE9172
39	80PORT / PWR SW / OV NCT3933
40	VIA VL800
41	TABLE LIST

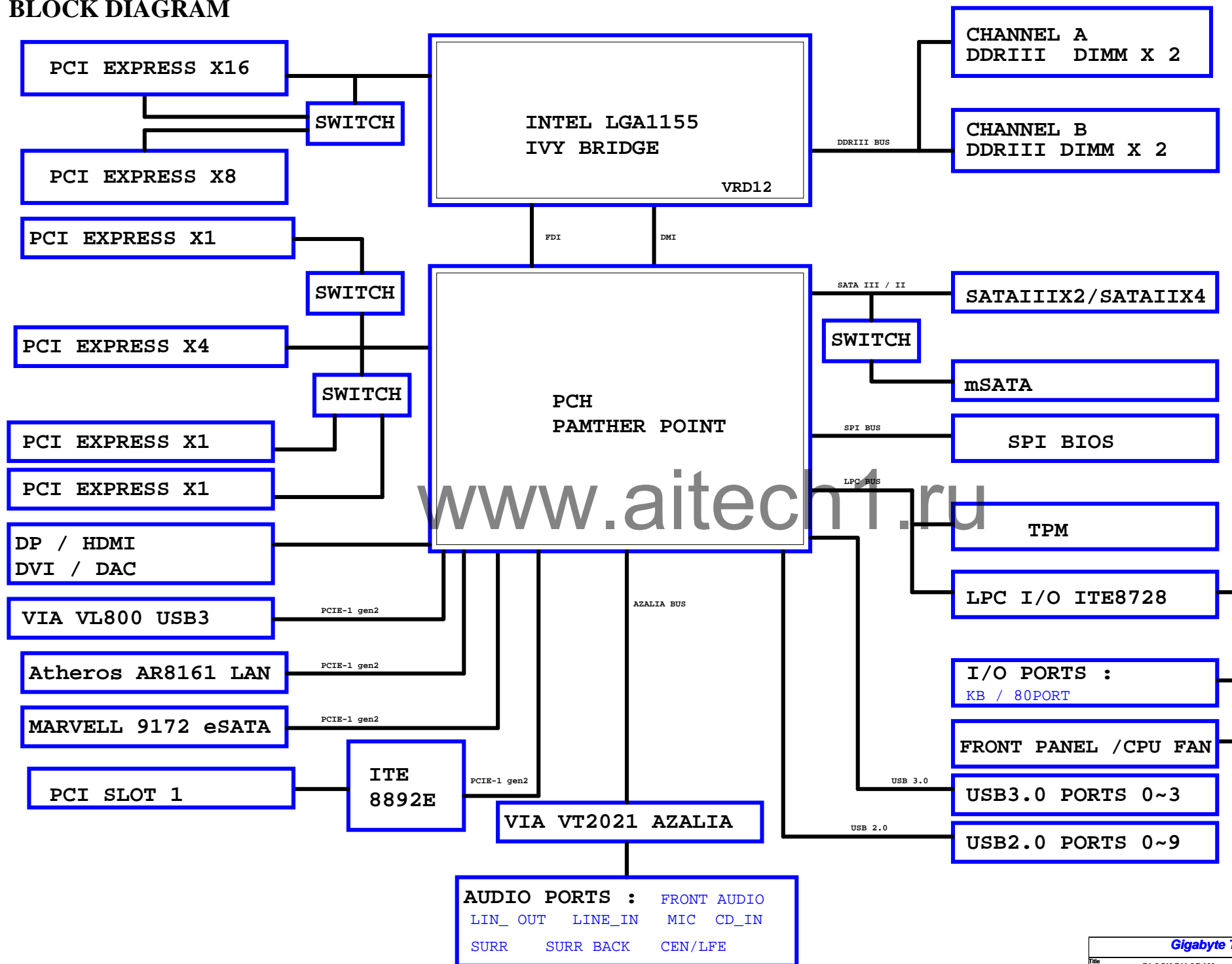


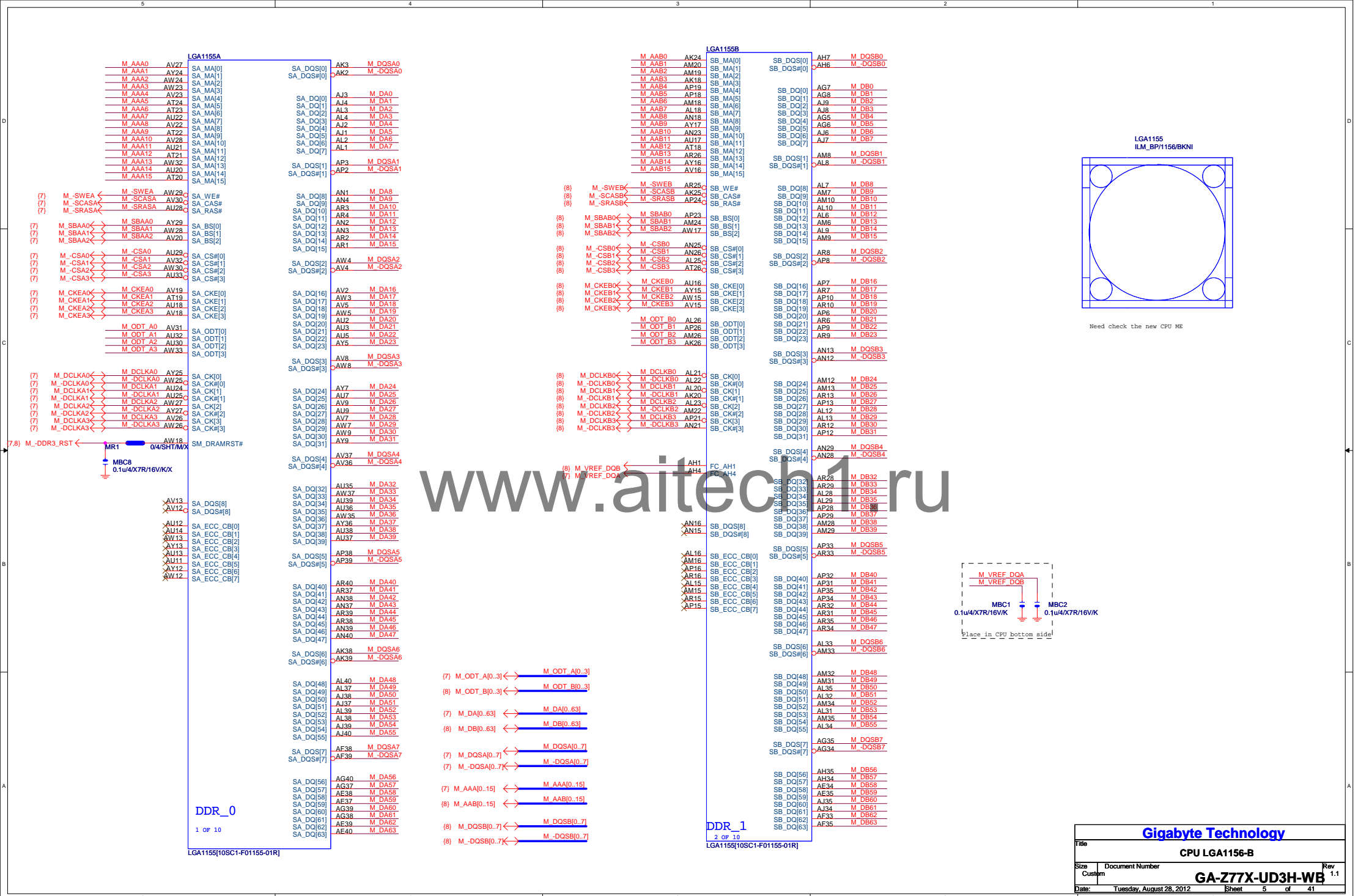
Component value change history

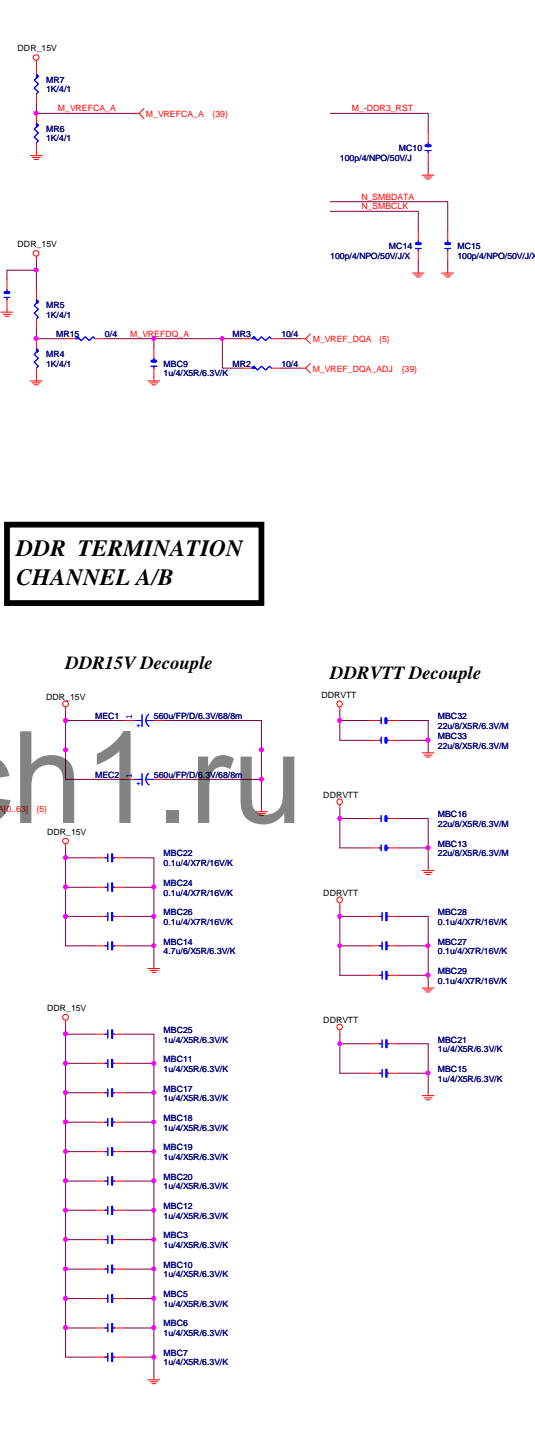
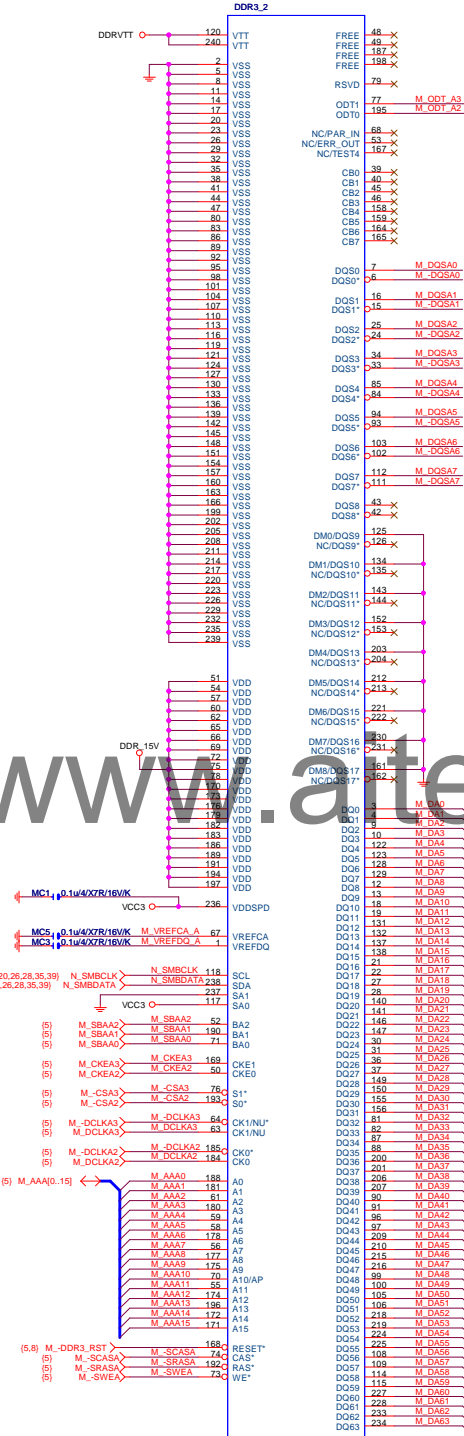
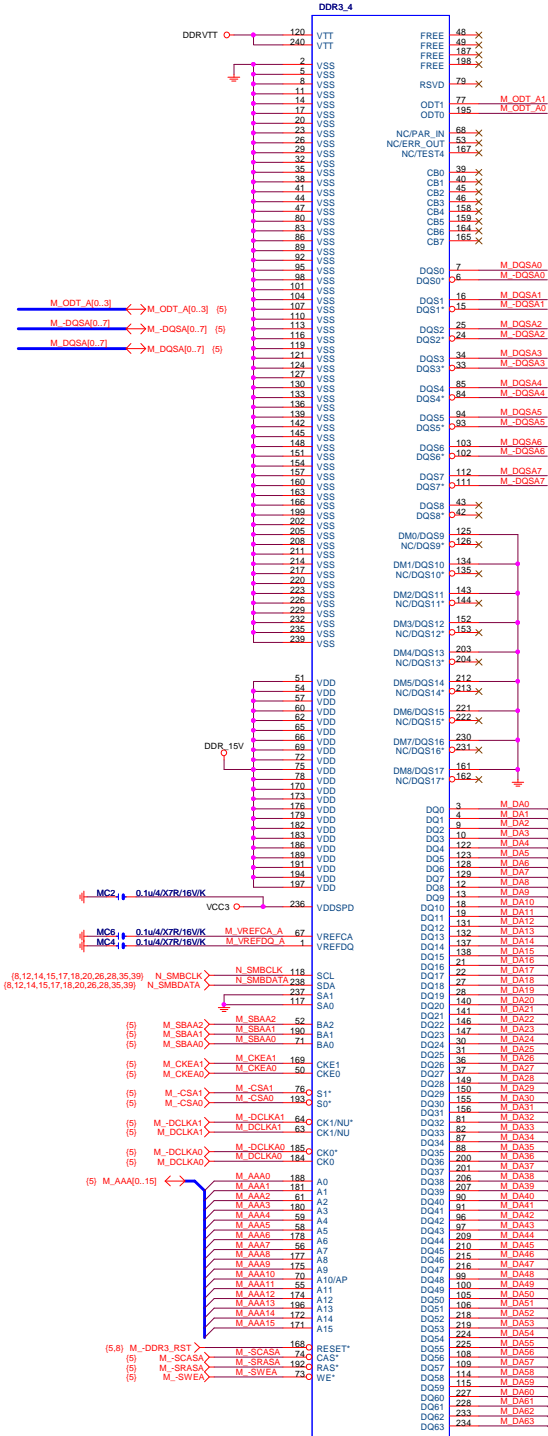
[illegible]

DATE	Change Item	Reason
2011/12/12	Add VIA VL800 USB3 PCIE X1_1 switch from PCIE X4 KB_USB3 , USB3_ESATA	Spec Change
2012/01/08	Add VR_HOT SCH MODIFY DDR15V POWER PLANE MODIFY IR8550 SCH	
2012/01/19	MODIFY FAN WORD RHU2 / CEC11 MASK MODIFY SW4 FOOTPRINT	
2012/02/10	0.36uH choke footprint CHOKE1U-30A-1P MAC61 footprint change from 0805 to 0603	
2012/03/14	DDR LAYOUT RULE CHANGE TO T	
2012/04/20	DDR LAYOUT RULE CHANGE SLOT GAP ADD DBC36 FOR CPUPWROK BY EMI	

BLOCK DIAGRAM

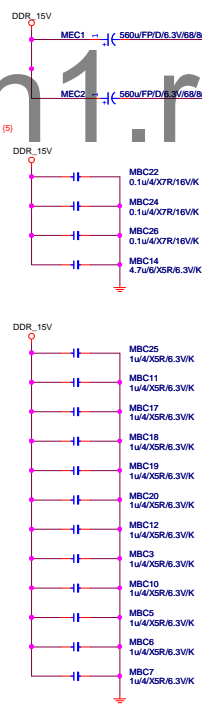




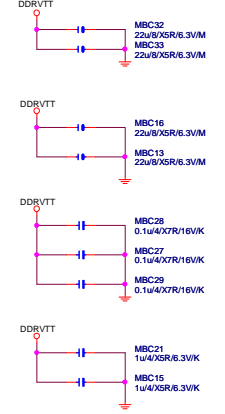


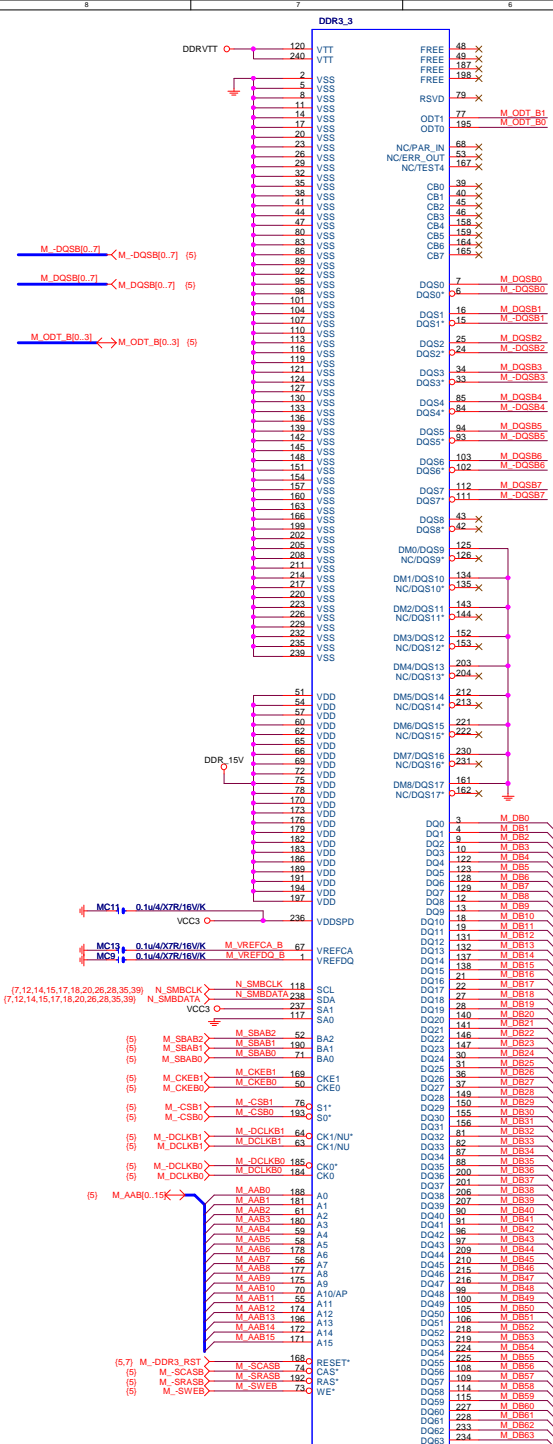
DDR TERMINATION CHANNEL A/B

DDR15V Decouple

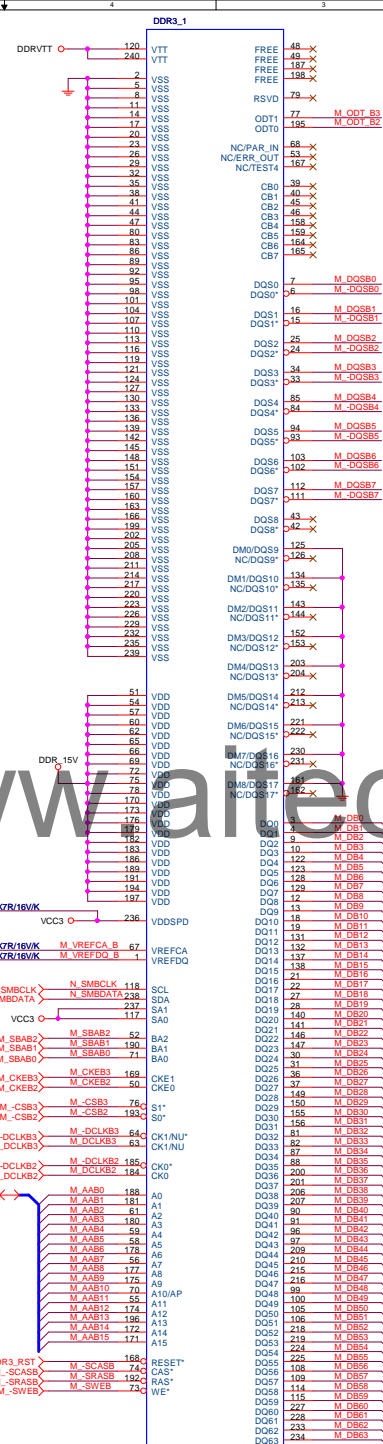


DDRVT Decouple

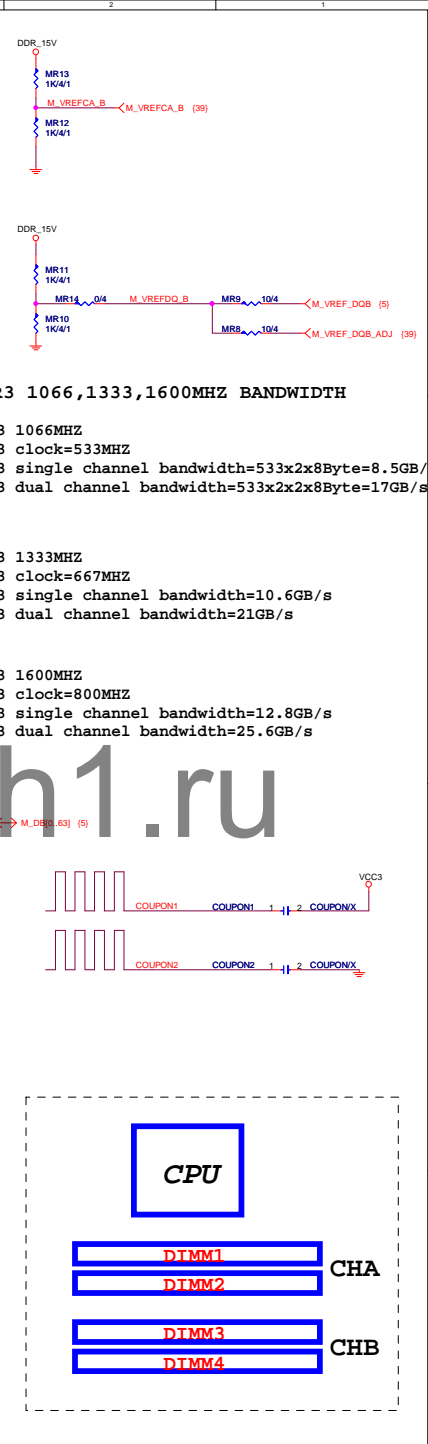




DDR3_3



DDR3_1

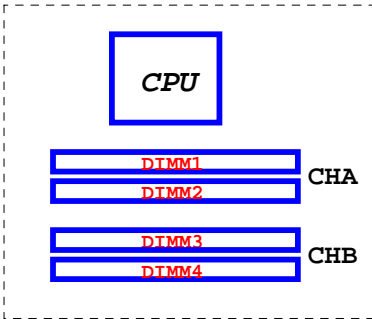


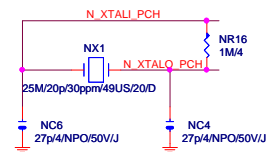
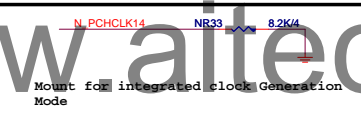
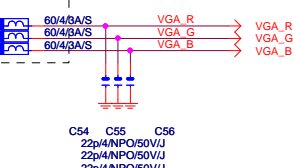
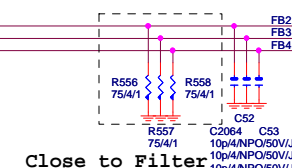
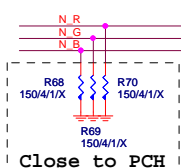
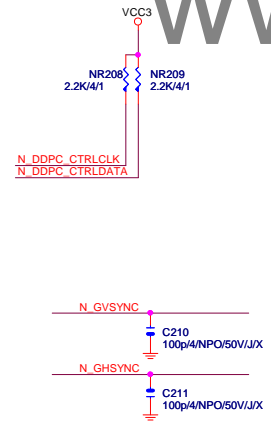
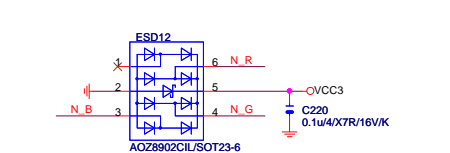
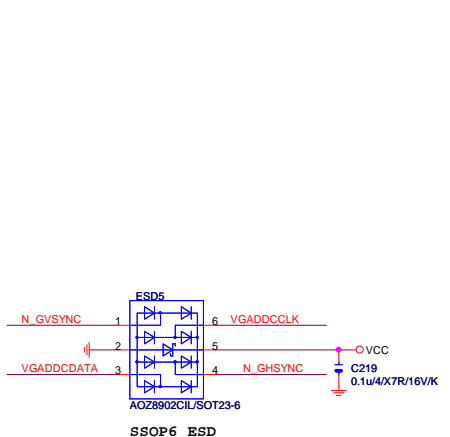
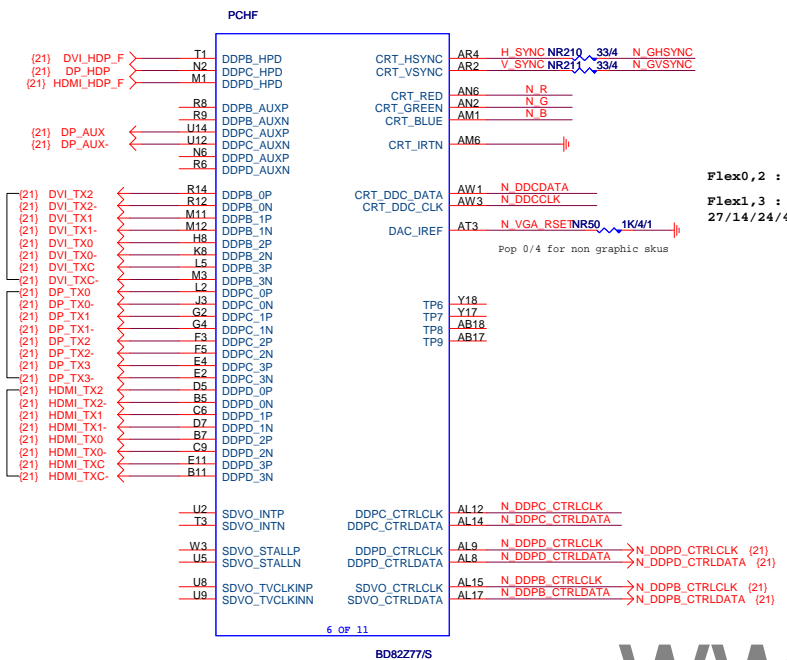
DDR3 1066,1333,1600MHZ BANDWIDTH

DDR3 1066MHZ
DDR3 clock=533MHZ
DDR3 single channel bandwidth=533x2x8Byte=8.5GB/s
DDR3 dual channel bandwidth=533x2x2x8Byte=17GB/s

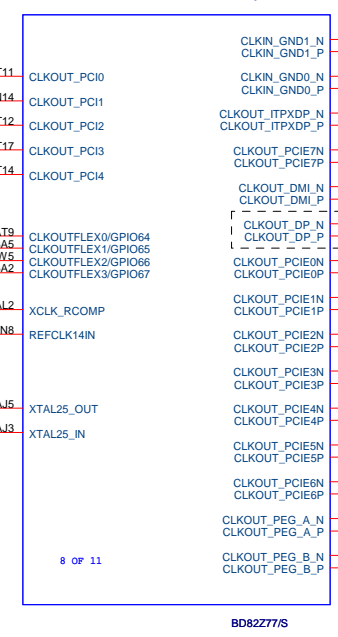
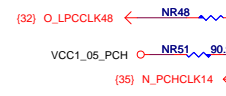
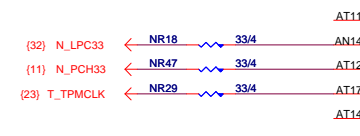
DDR3 1333MHZ
DDR3 clock=667MHZ
DDR3 single channel bandwidth=10.6GB/s
DDR3 dual channel bandwidth=21GB/s

DDR3 1600MHZ
DDR3 clock=800MHZ
DDR3 single channel bandwidth=12.8GB/s
DDR3 dual channel bandwidth=25.6GB/s

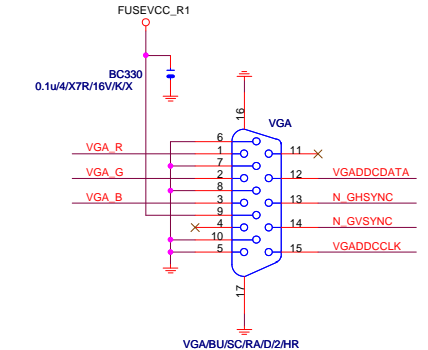
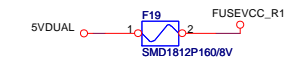




Flex0,2 : 33MHZ
Flex1,3 : 27/14/24/48/25MHZ



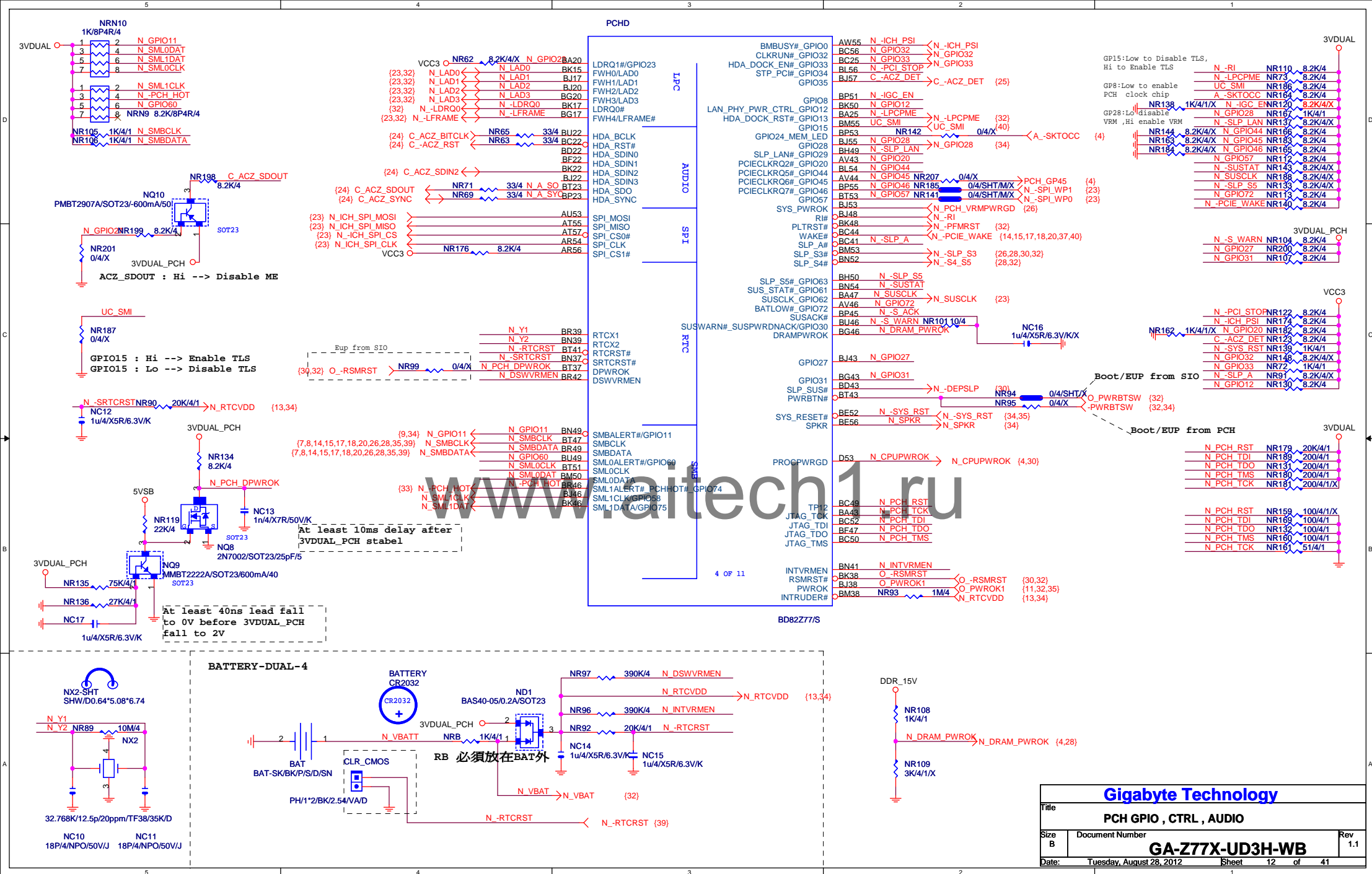
Differential Clock:18/6/4/6/18
Impedance=90 +- 15%

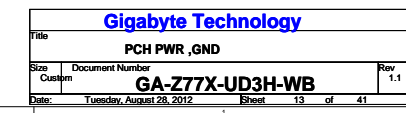


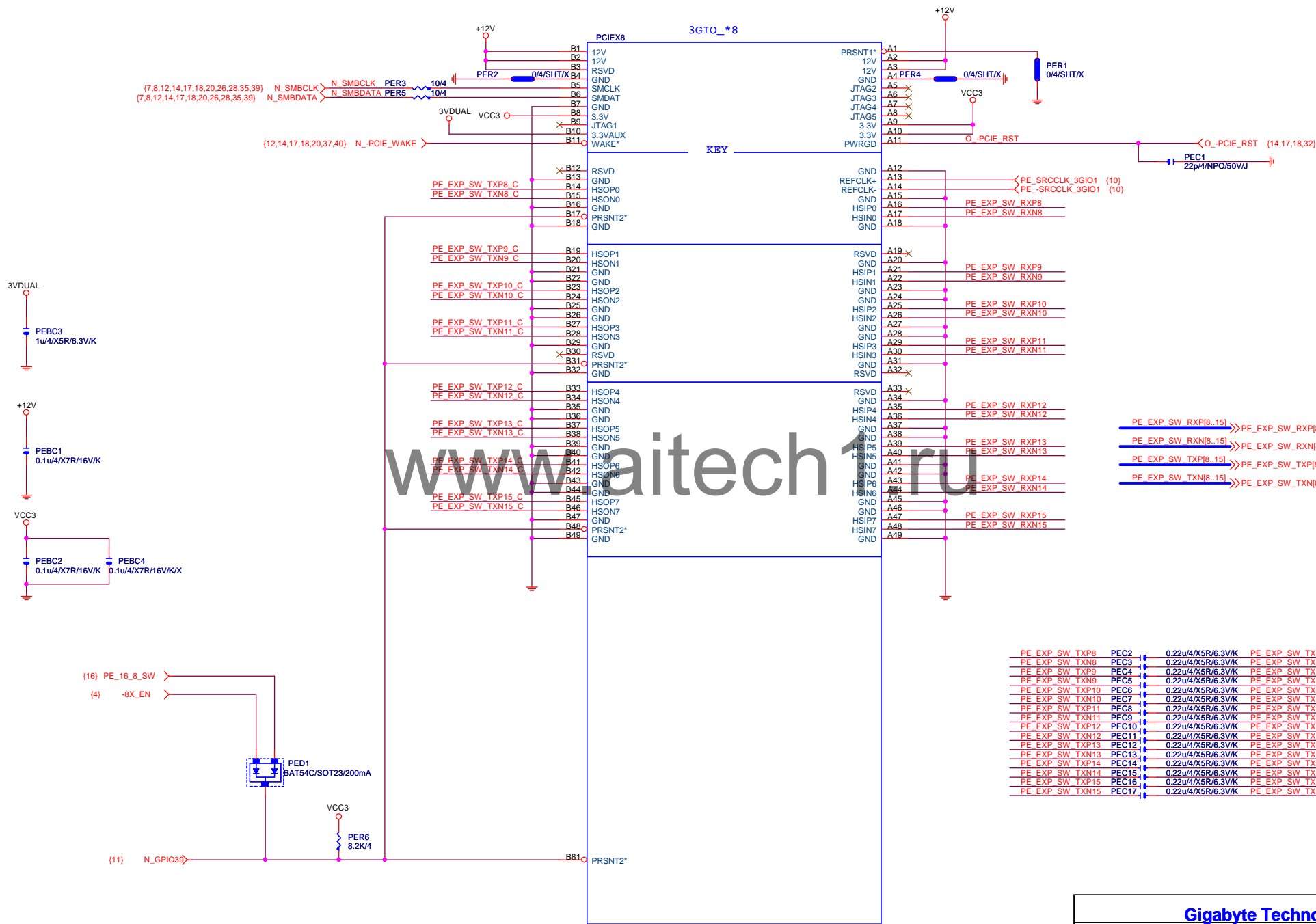
Gigabyte Technology			
Title			
PCH DISPLAY ,CLK BUFFER			
Size	Document Number	Rev	
Custom	GA-Z77X-UD3H-WB	1.1	
Date:	Tuesday, August 28, 2012	Sheet	10 of 41

PCHC

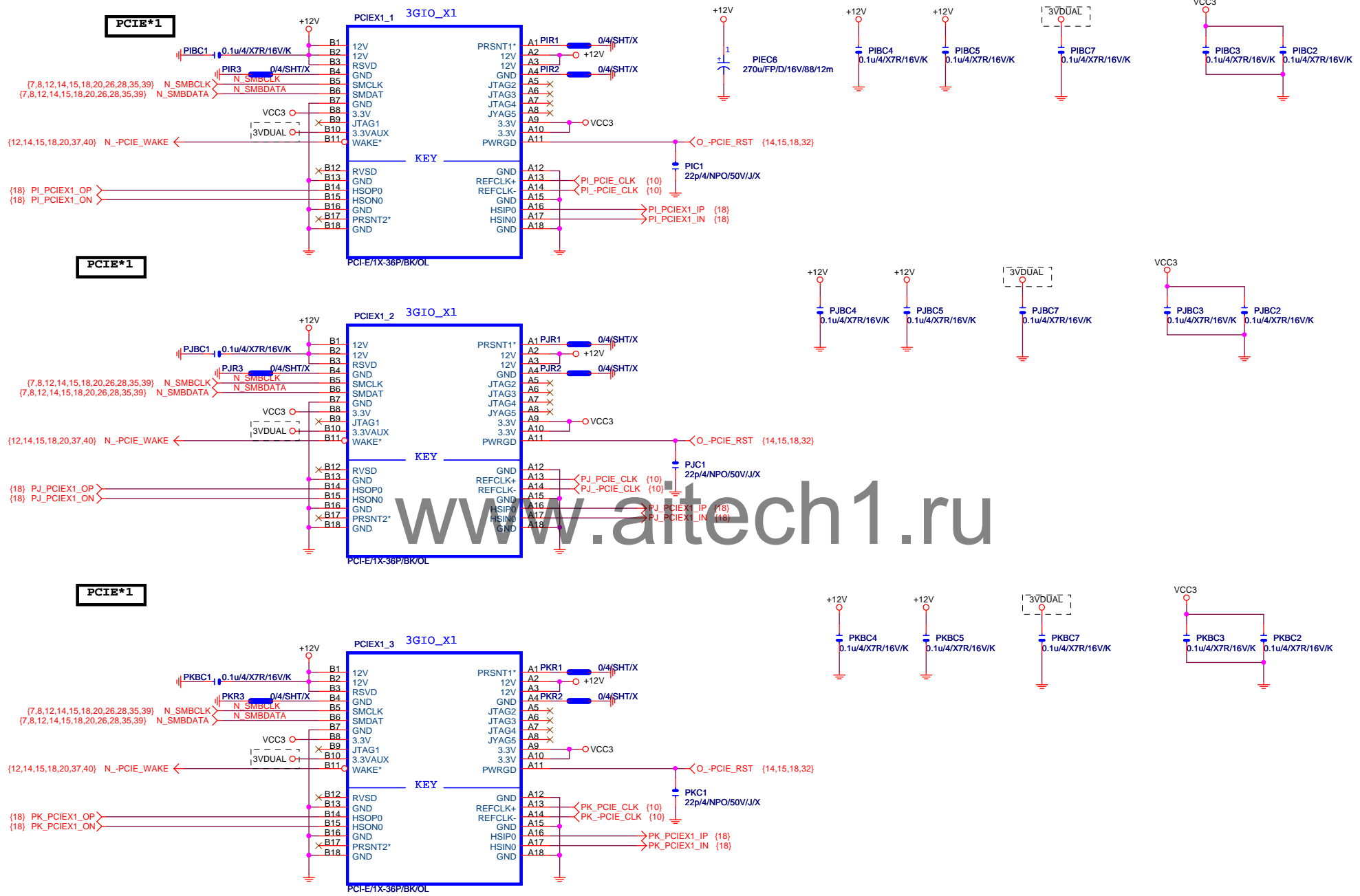








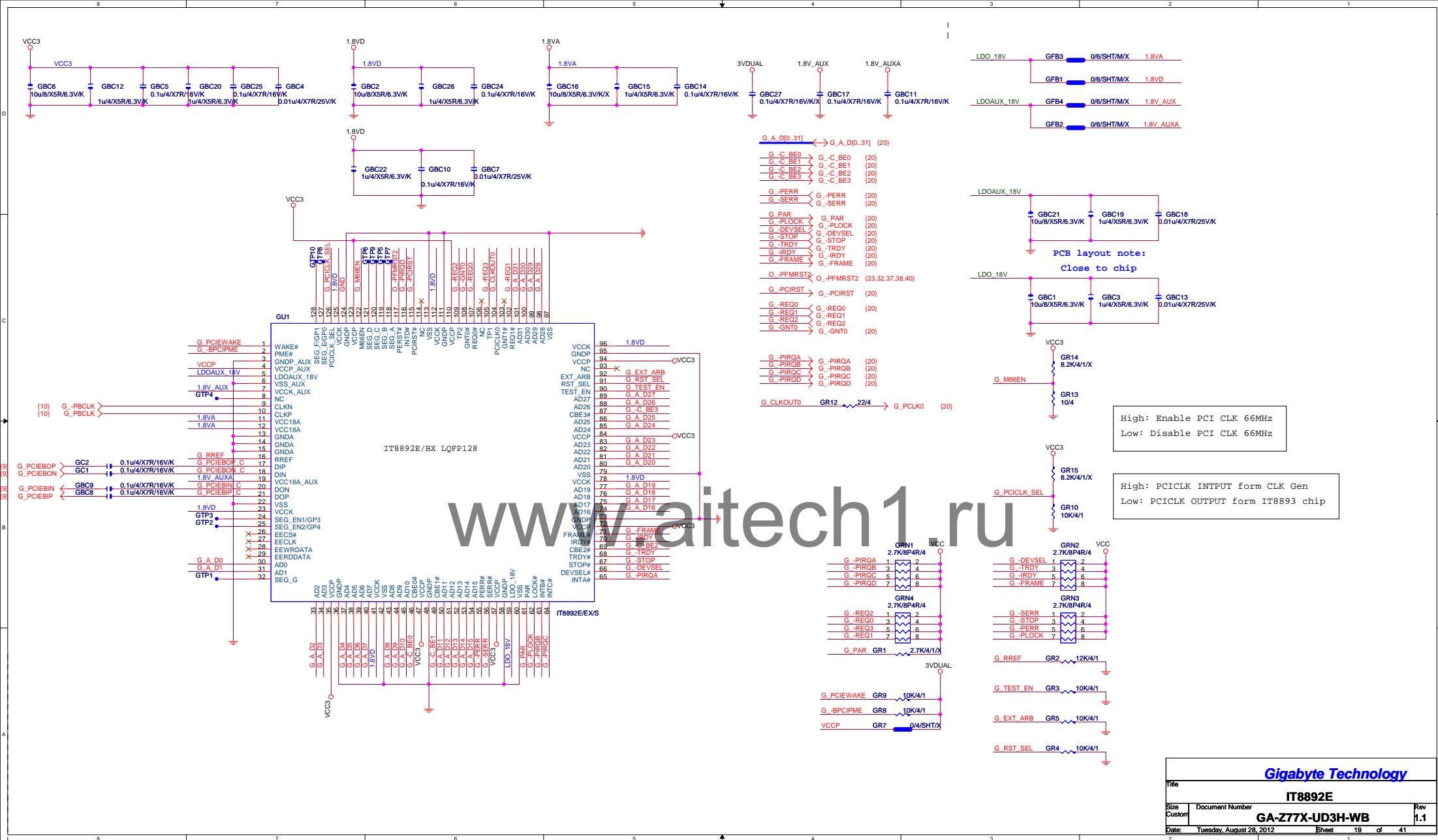
PE EXP SW TXP8	PEC2	0.22u4/X5R/6.3V/K	PE EXP SW TXP8 C
PE EXP SW TXN8	PEC3	0.22u4/X5R/6.3V/K	PE EXP SW TXN8 C
PE EXP SW TXP9	PEC4	0.22u4/X5R/6.3V/K	PE EXP SW TXP9 C
PE EXP SW TXN9	PEC5	0.22u4/X5R/6.3V/K	PE EXP SW TXN9 C
PE EXP SW TXP10	PEC6	0.22u4/X5R/6.3V/K	PE EXP SW TXP10 C
PE EXP SW TXN10	PEC7	0.22u4/X5R/6.3V/K	PE EXP SW TXN10 C
PE EXP SW TXP11	PEC8	0.22u4/X5R/6.3V/K	PE EXP SW TXP11 C
PE EXP SW TXN11	PEC9	0.22u4/X5R/6.3V/K	PE EXP SW TXN11 C
PE EXP SW TXP12	PEC10	0.22u4/X5R/6.3V/K	PE EXP SW TXP12 C
PE EXP SW TXN12	PEC11	0.22u4/X5R/6.3V/K	PE EXP SW TXN12 C
PE EXP SW TXP13	PEC12	0.22u4/X5R/6.3V/K	PE EXP SW TXP13 C
PE EXP SW TXN13	PEC13	0.22u4/X5R/6.3V/K	PE EXP SW TXN13 C
PE EXP SW TXP14	PEC14	0.22u4/X5R/6.3V/K	PE EXP SW TXP14 C
PE EXP SW TXN14	PEC15	0.22u4/X5R/6.3V/K	PE EXP SW TXN14 C
PE EXP SW TXP15	PEC16	0.22u4/X5R/6.3V/K	PE EXP SW TXP15 C
PE EXP SW TXN15	PEC17	0.22u4/X5R/6.3V/K	PE EXP SW TXN15 C



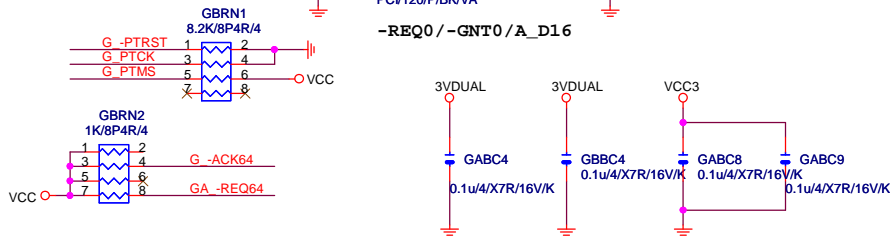
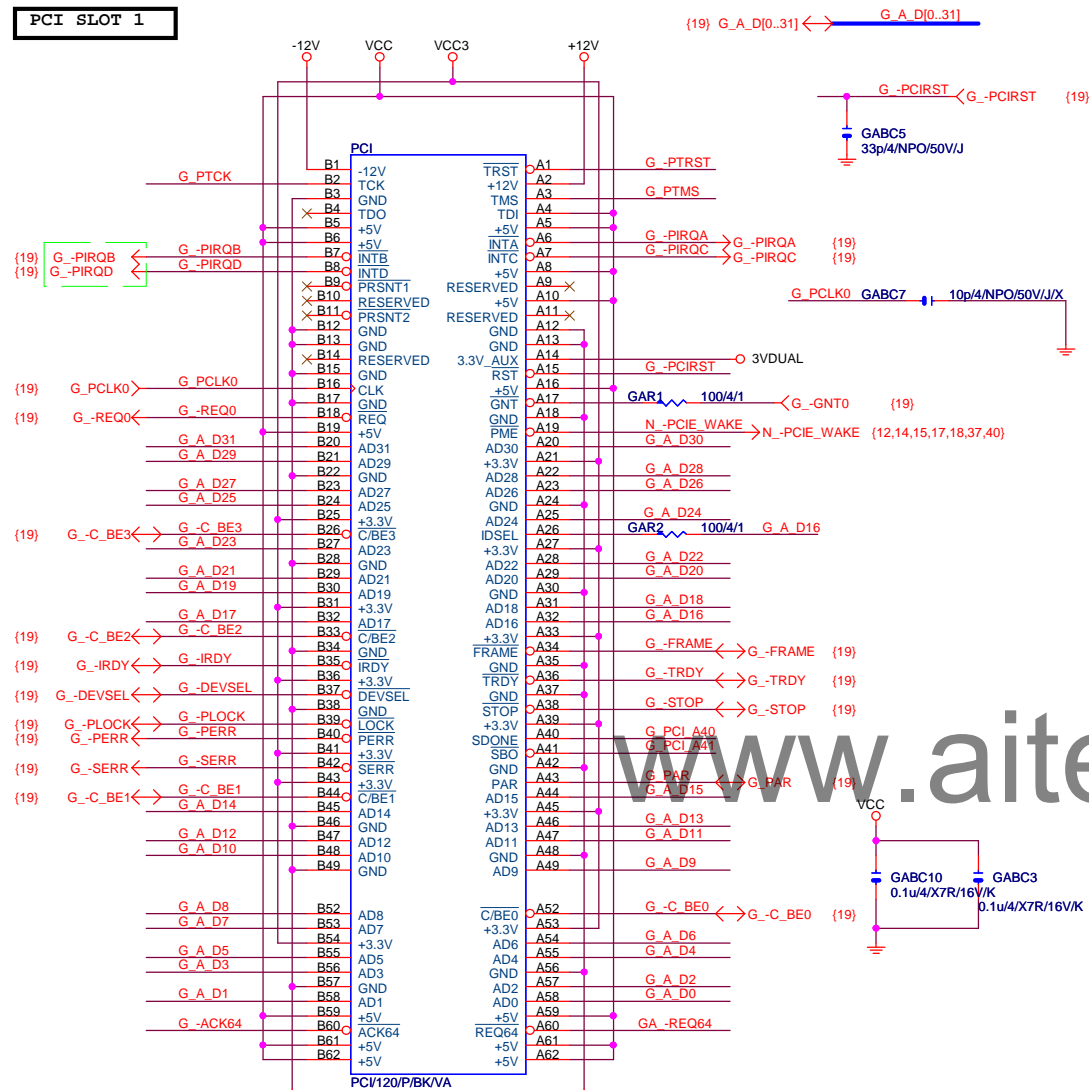
PCIE*4



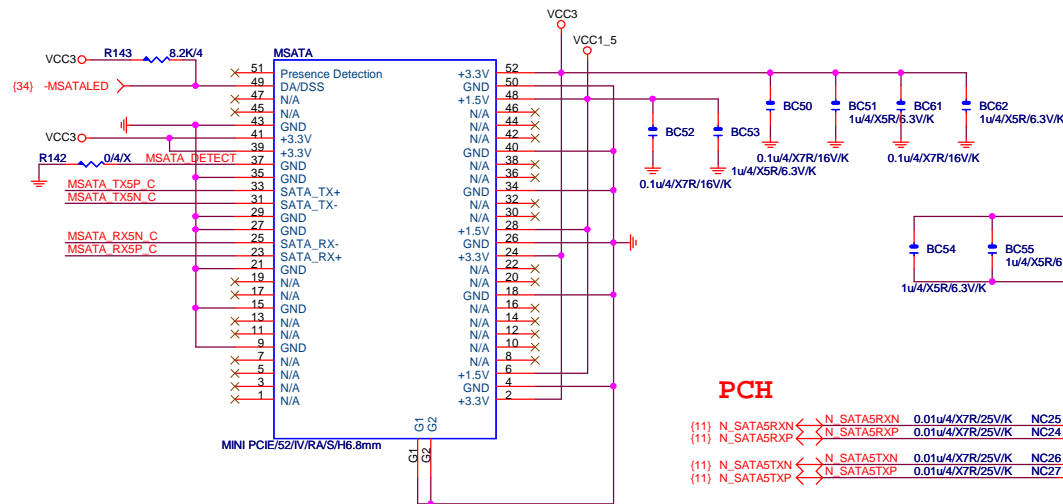
GIGABYTE™			
Title			
PCI_E_X4			
Size	Document Number		Rev
Custom	GA-Z77X-UD3H-WB		1.1
Date:	Tuesday, August 28, 2012	Sheet	18 of 41



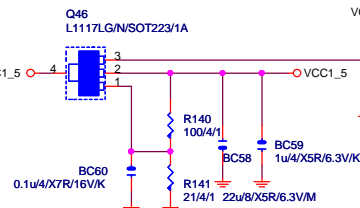
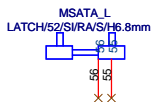
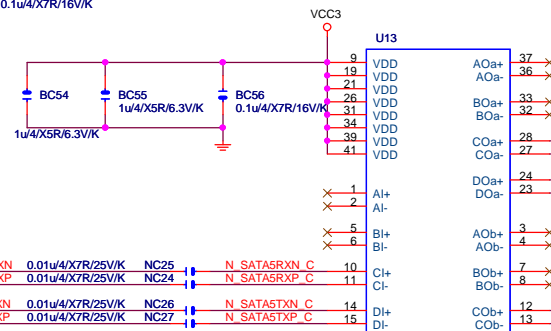
PCI SLOT 1



GIGABYTE™			
Title			
PCI SLOT 1			
Size	Document Number	Rev	
Custom	GA-Z77X-UD3H-WB	1.1	
Date:	Tuesday, August 28, 2012	Sheet	20 of 41



N_SATA5RXN C R134 0/4/X N_SATA5RXNC
 N_SATA5RXP C R136 0/4/X N_SATA5RXPC
 N_SATA5TXN C R137 0/4/X N_SATA5TXNC
 N_SATA5TXP C R139 0/4/X N_SATA5TXPC
FIX PCH-SATA --> SATA5
R請放在U13背面



www.gitech1.ru

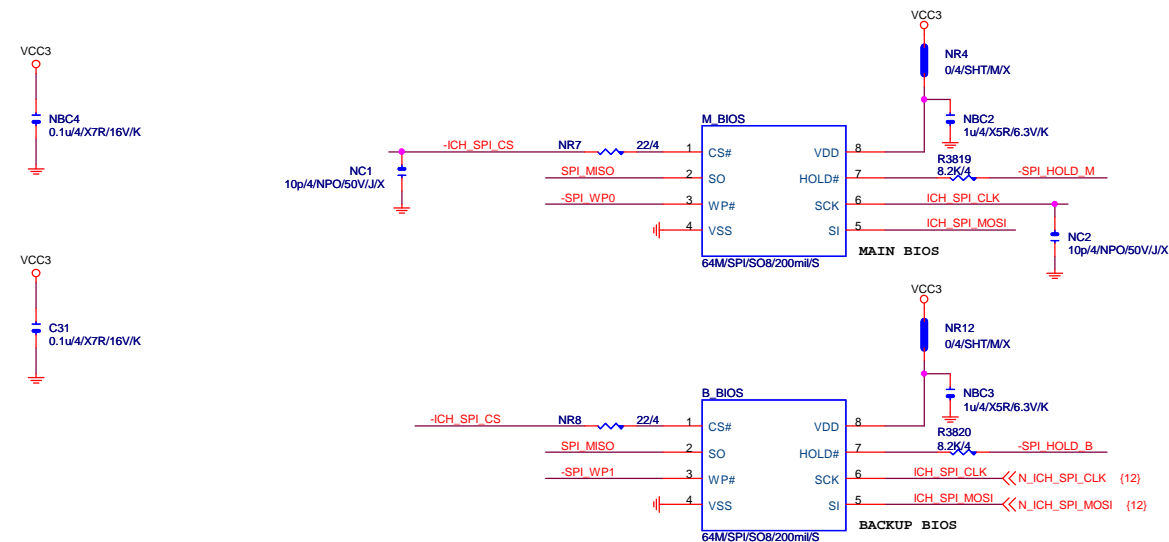
SATA2 port5

mSATA

Function	SEL
xI--> xOa	L
xI--> xOb	H

GIGABYTE™

Title mSATA Conn		
Size Custom	Document Number GA-Z77X-UD3H-WB	Rev 1.1
Date: Tuesday, August 28, 2012	Sheet 22	of 41



MOSI For DMI RX Termination Voltage

(12) N_ICH_SPI_MOSI << ICH_SPI_MOSI NR10 8.2K/4/X
(12) N_ICH_SPI_CS << ICH_SPI_CS NR9 8.2K/4/X
(12) N_ICH_SPI_HOLD0 << ICH_SPI_HOLD0 NR3 8.2K/4/X
(12) N_ICH_SPI_HOLD1 << ICH_SPI_HOLD1 NR11 8.2K/4/X

(12) N_-SPI_WP1 << -SPI_WP1 NR2 8.2K/4/X
(12) N_-SPI_WP0 << -SPI_WP0 NR1 8.2K/4/X
(12) N_ICH_SPI_MISO << ICH_SPI_MISO NR5 8.2K/4

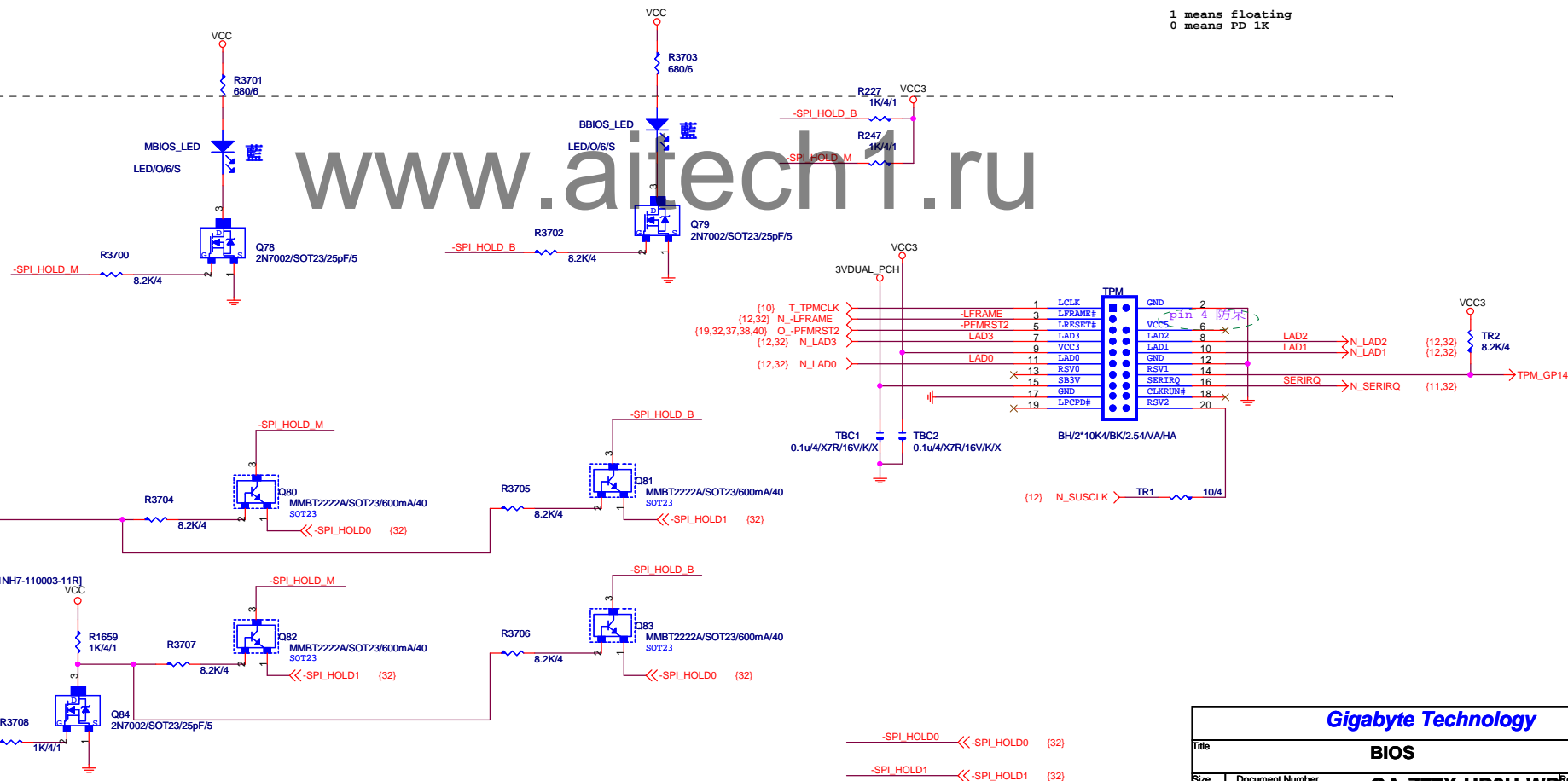
(11) N_-GNT0 << NR26 1K/4/1/X
(11) N_-GNT1 << NR25 1K/4/1/X

Default int pull up

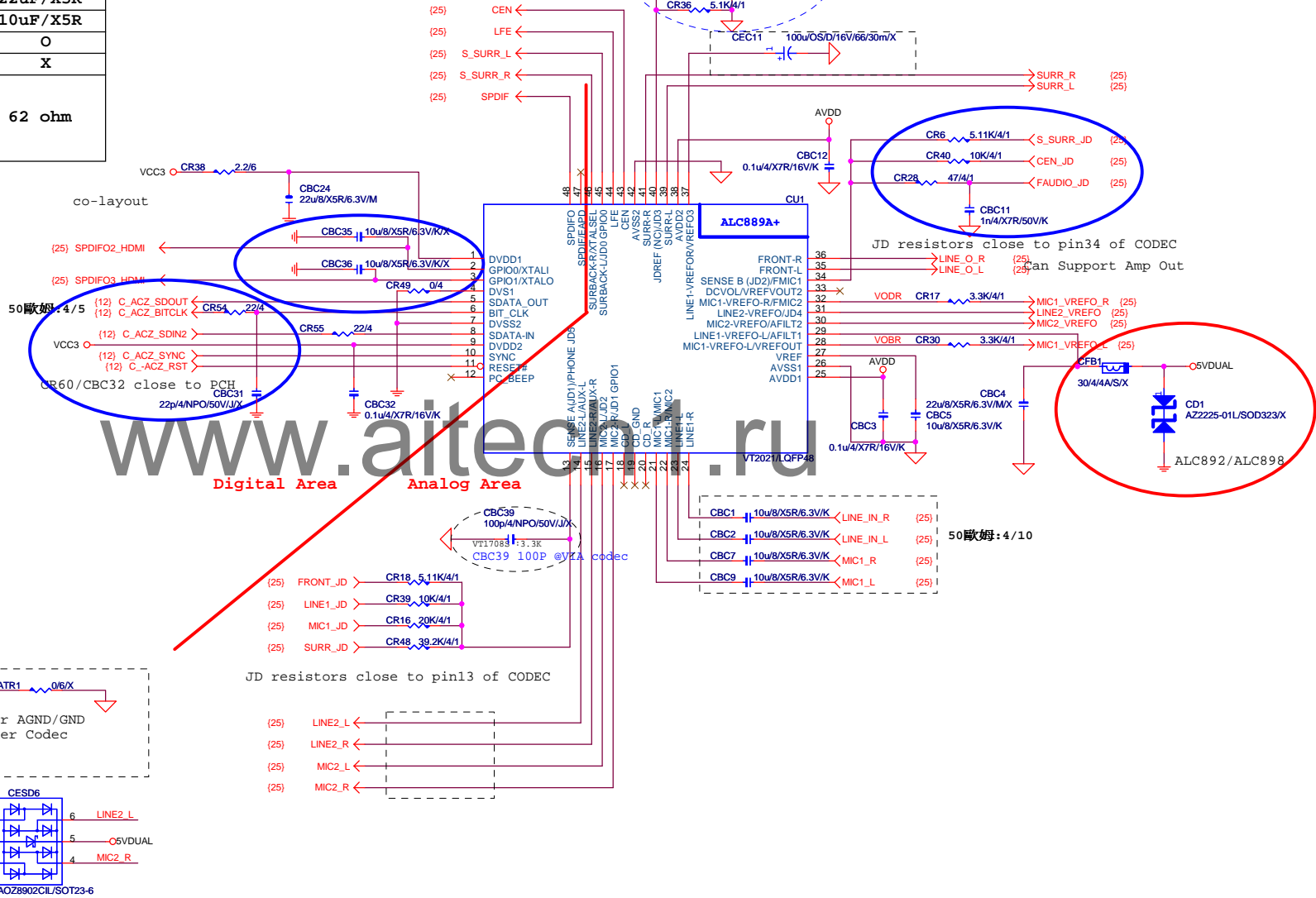
SPI_MISO NR6 22/4 << N_ICH_SPI_MISO (12)

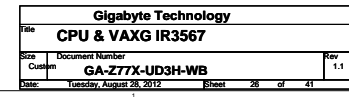
BOOT DEVICE	GNT0	GNT1
LPC	0	0
PCI	0	1
NAND	1	0
SPI	1	1

1 means floating
0 means PD 1K

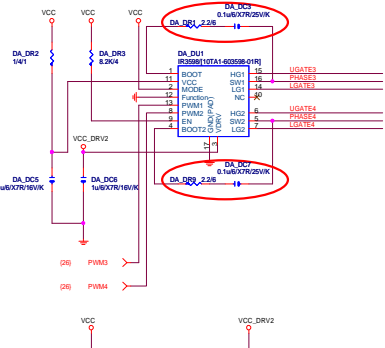


	ALC889	ALC889B	ALC898/ALC892
CR49	O	O	X
CBC36	X	X	10uF/X5R
CBC35	X	10uF/X5R	X
CR52	O	X	O
CR53	X	O	X
CBC1/CBC2	22uF/X5R	22uF/X5R	22uF/X5R
CBC7/CBC9/CBC20/CBC15	10uF/X5R	10uF/X5R	10uF/X5R
CFB1/CD1/CBC4	X	X	O
CD2/CD3/CQ3/CQ4	O	O	X
CR7/CR9/CR5/CR13/ CR29/CR32/CR46/CR19/ CR50/CR41/CR21/CR47/ CR2/CR11/CR14/CR24	62 ohm	62 ohm	62 ohm





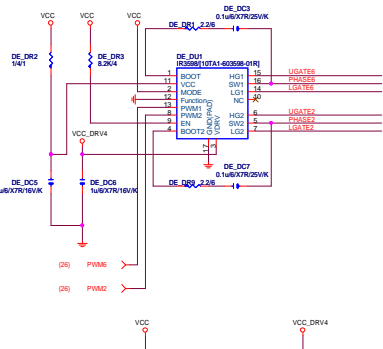
VCORE Phase 3,6



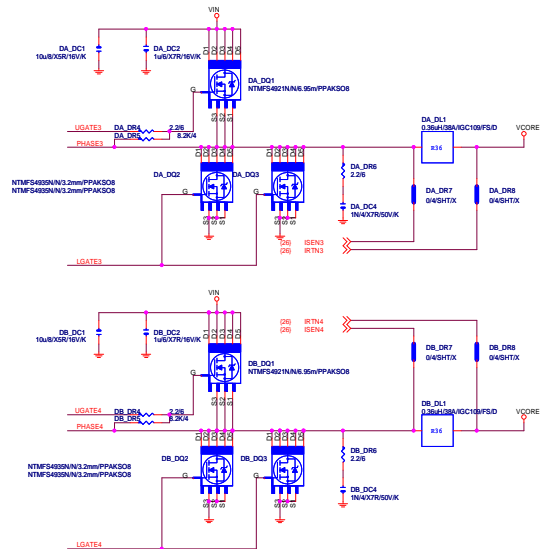
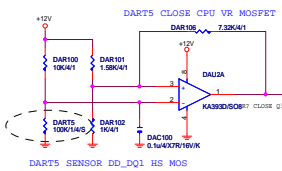
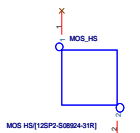
FUNCTION	MODE	PWM MODE	PHASE MODE
0	1	IR ATL	DUAL
1	1	IR ATL	Doubler
0	0	Tri-Seate	DUAL
1	0	Tri-Seate	Doubler
OPEN	0	Tri-Seate	Quad
OPEN	1	IR ATL	Quad

In Quad mode , IC1 pin10 link to IC2 pin10
IC1 pin9 link to IC2 pin9 without PU

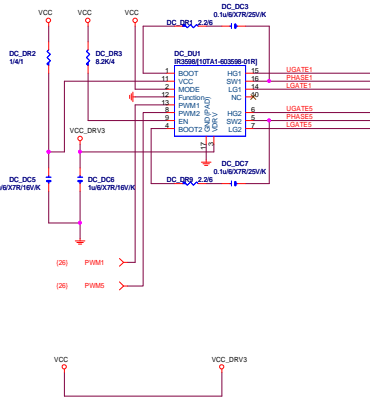
VCORE Phase 5,2



MOS HEATSINK



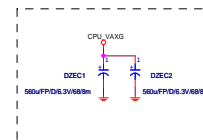
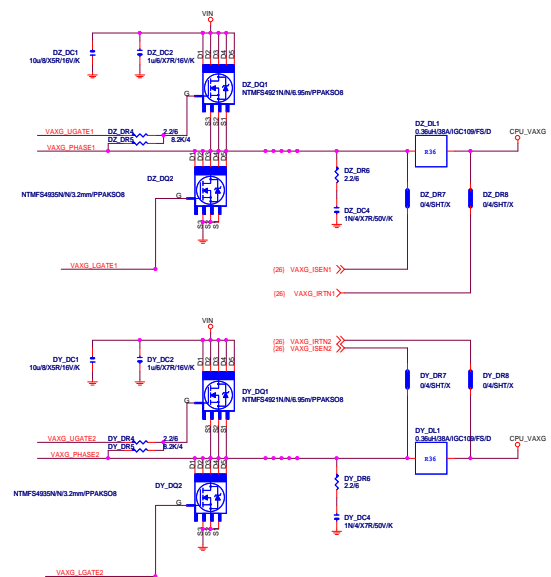
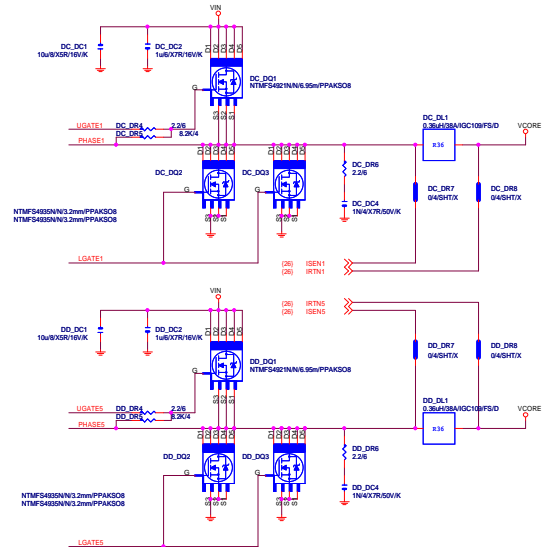
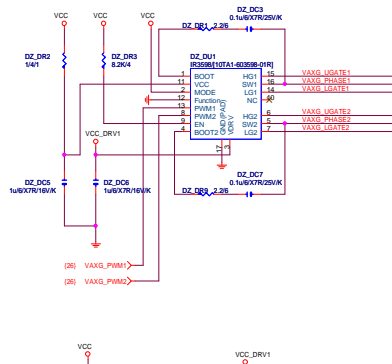
VCORE Phase 1,4

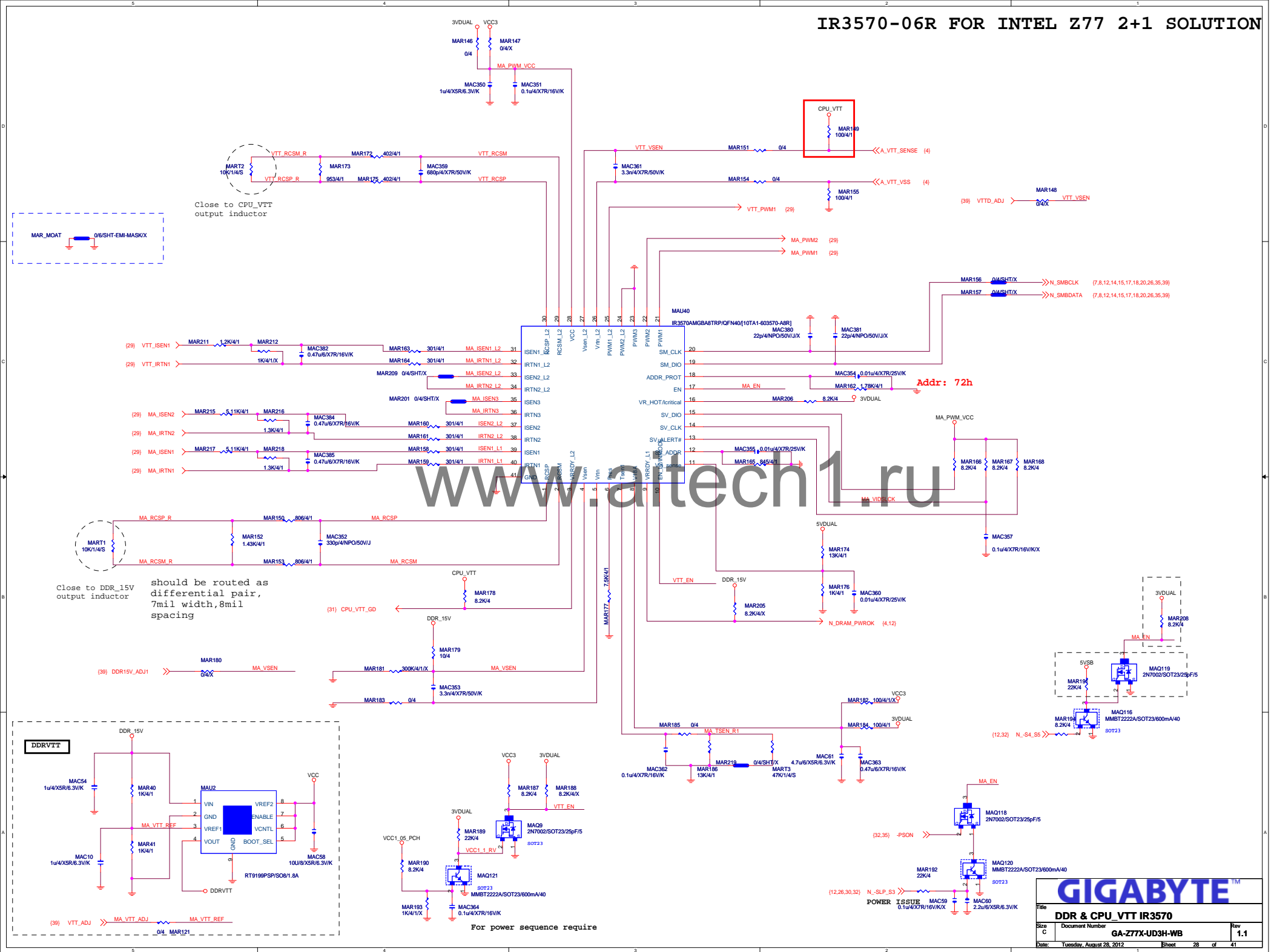


FUNCTION	MODE	PROG MODE	PHASE MODE
0	1	IR ATL	DUAL
1	1	IR ATL	Doubler
0	0	Tri-Sense	DUAL
1	0	Tri-Sense	Doubler
OPEN	0	Tri-Sense	Quad
OPEN	1	IR ATL	Quad

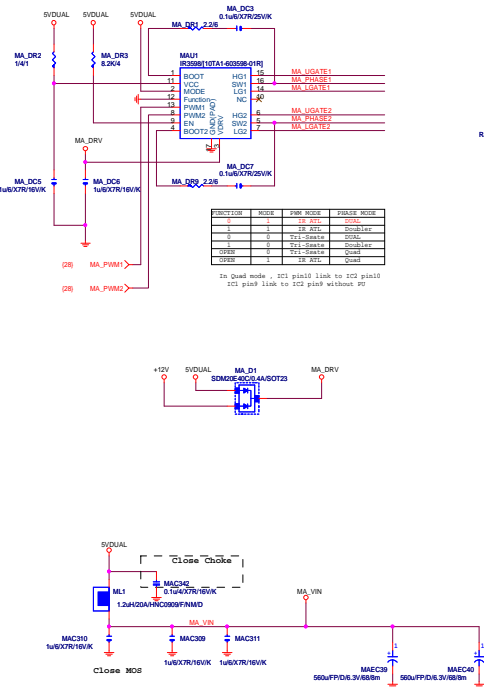
In Quad mode , IC1 pin10 link to IC2 pin1
IC1 pin9 link to IC2 pin9 without PU

VAXG Phase

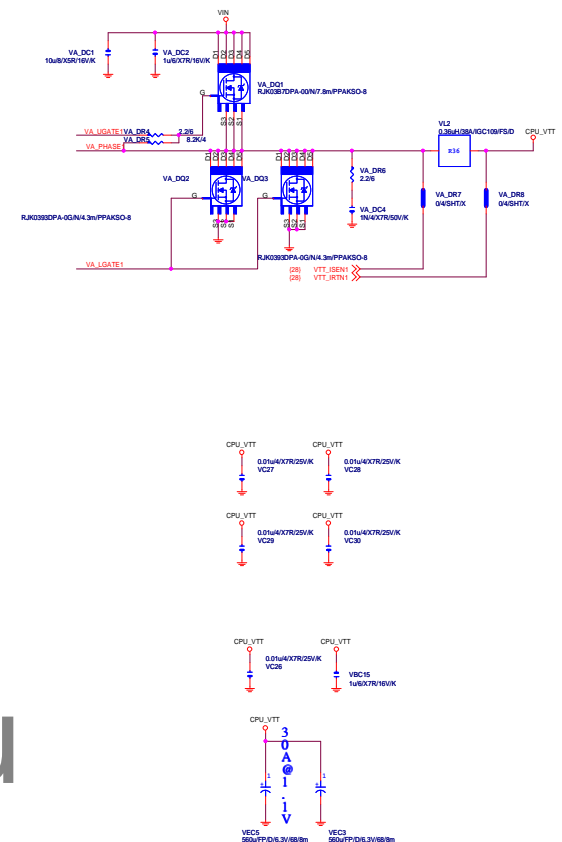
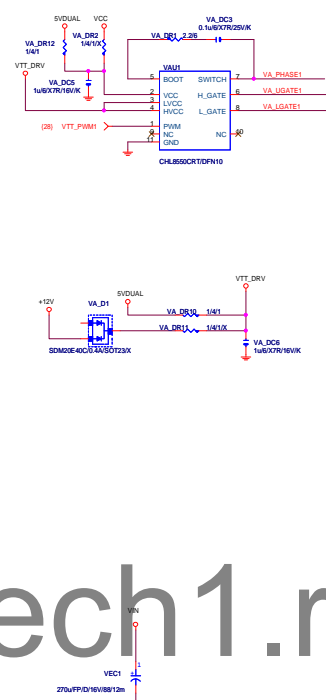




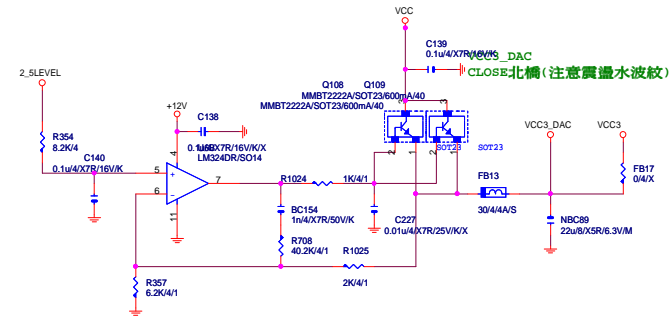
DDR_15V



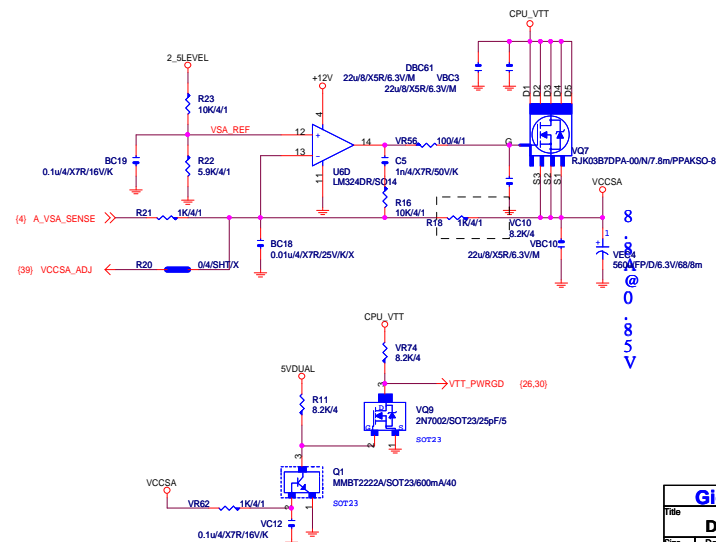
CPU_VTT

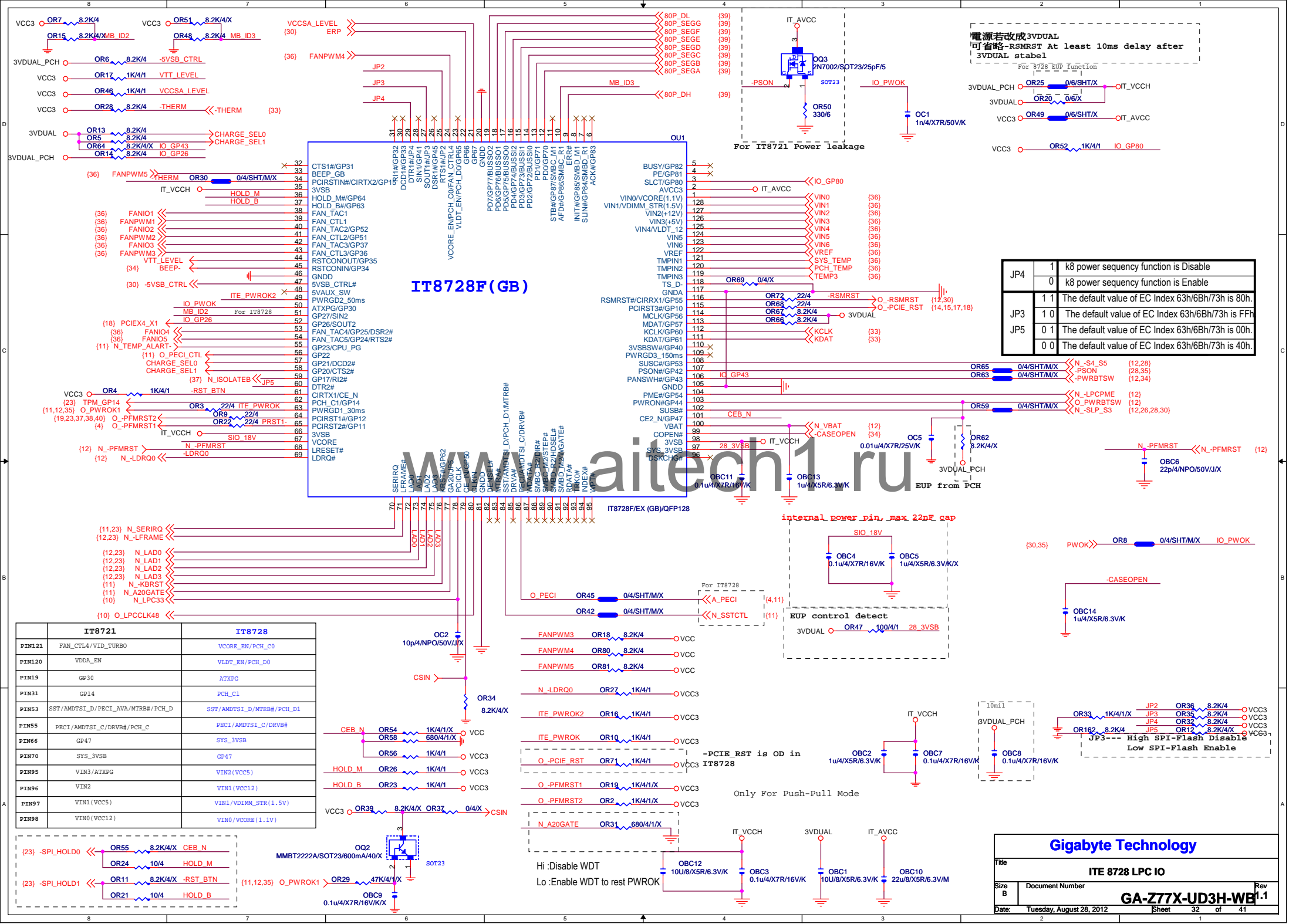


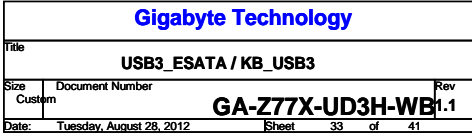
www.aitech1.ru

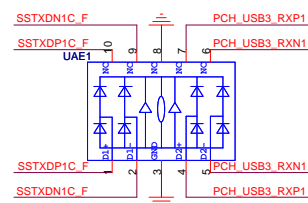
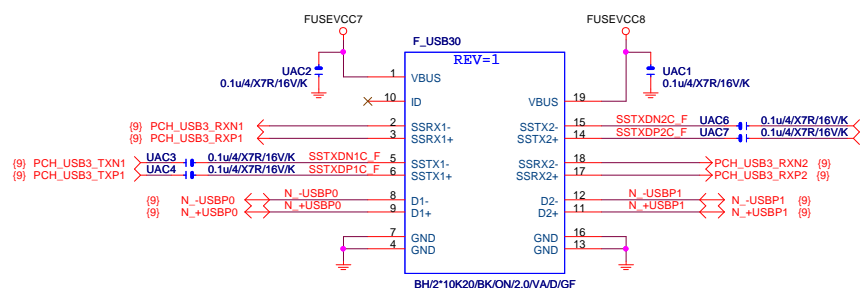
$$(3.3V/70mA+360\mu A)$$


www.aitech1.ru

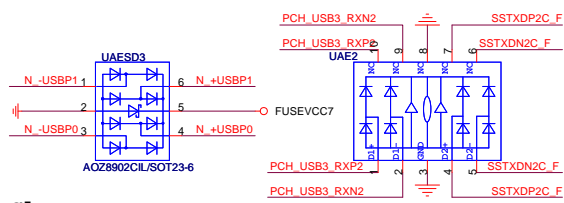






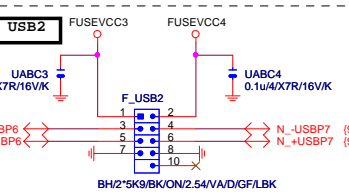
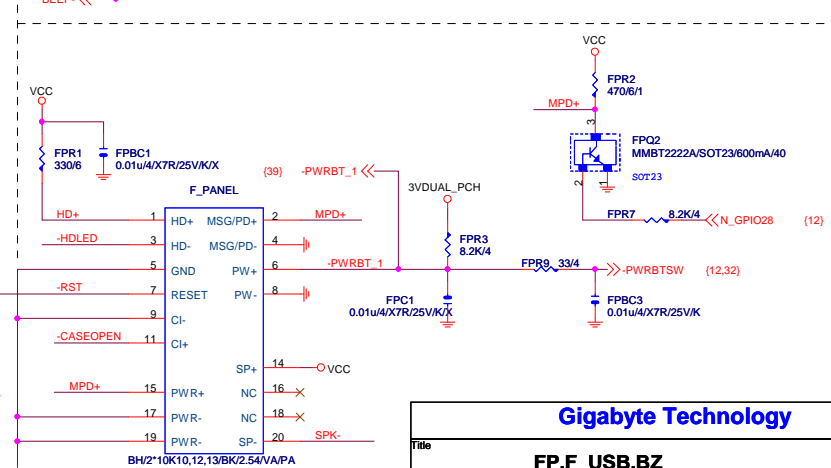
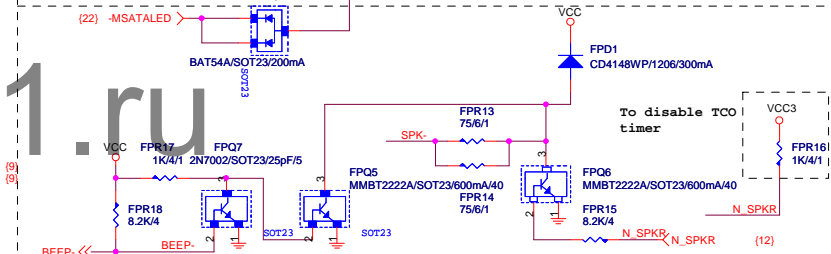
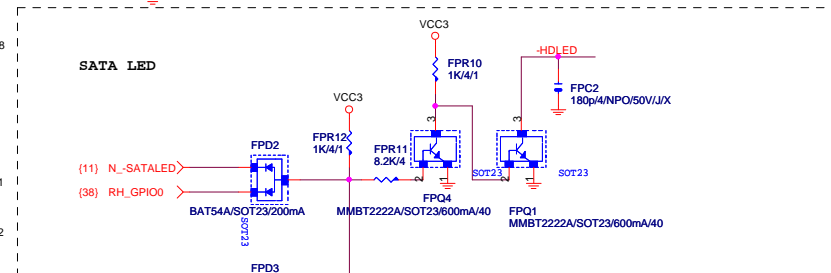
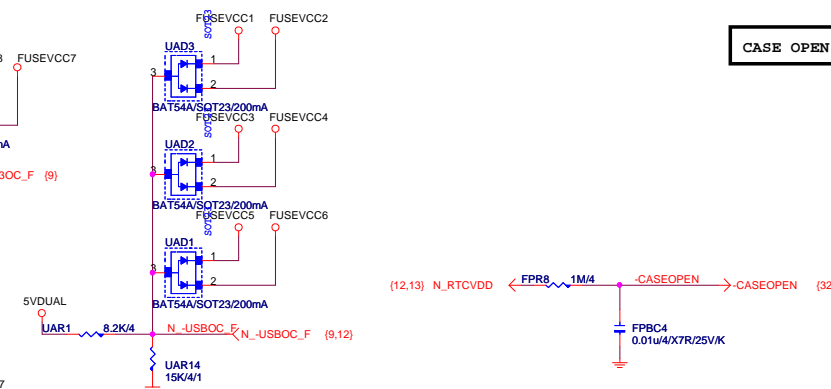
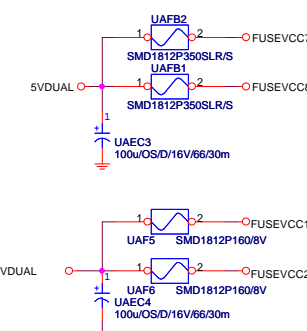
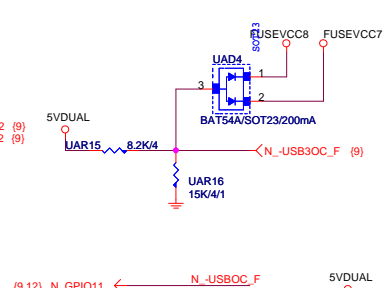


Close to connector

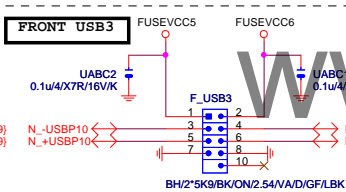


Close to connector

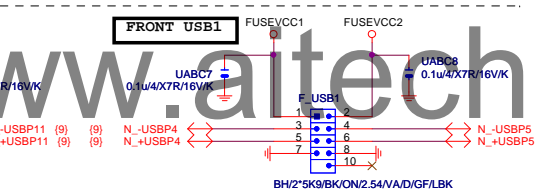
Close to connector



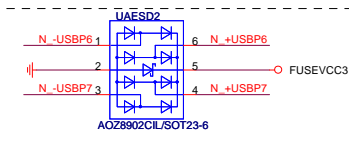
Close to connector



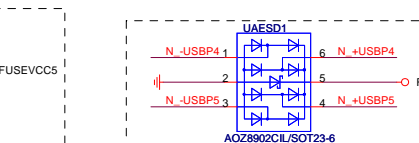
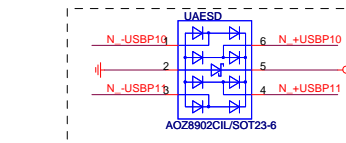
Close to connector



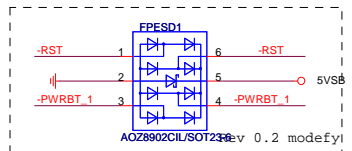
Close to connector



POWER PROTECT

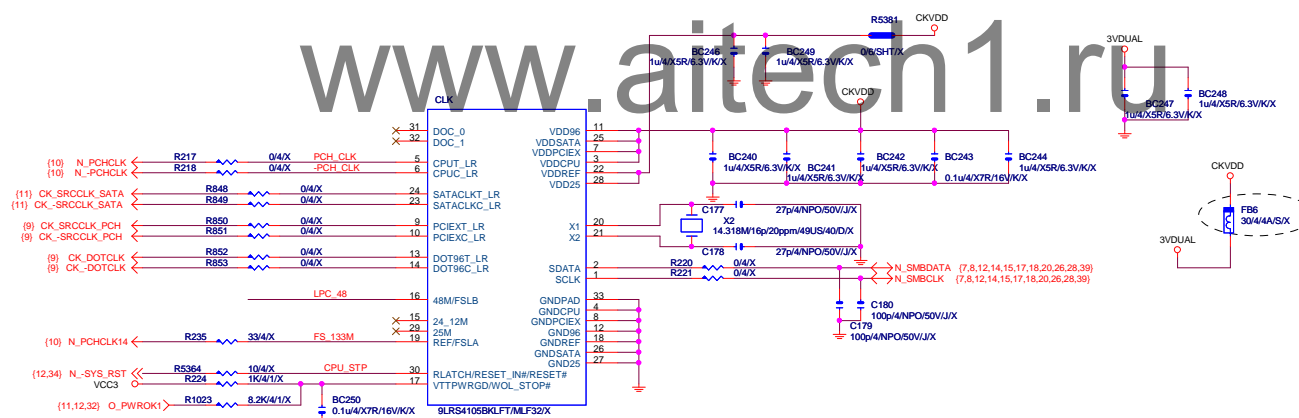
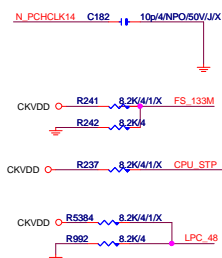


Close to connector

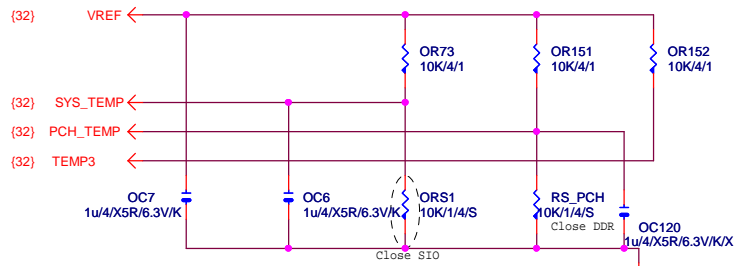


CPU Frequency Selection

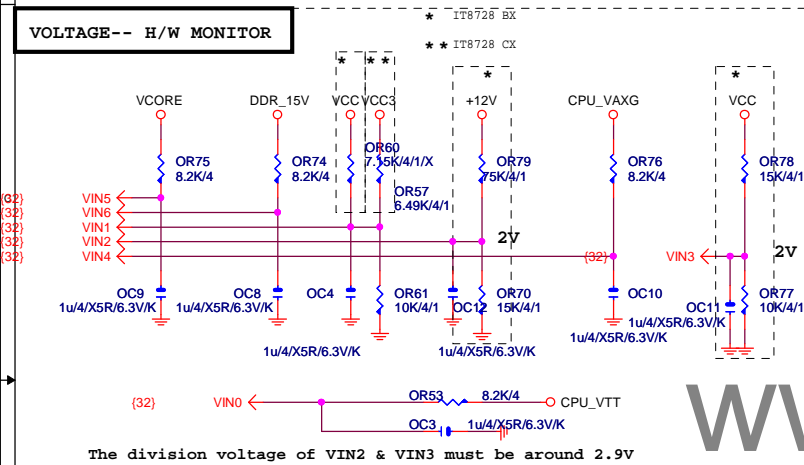
FSLB	FSLA	CPU
0	0	100M <Default>
0	1	133M
1	0	200M
1	1	166M



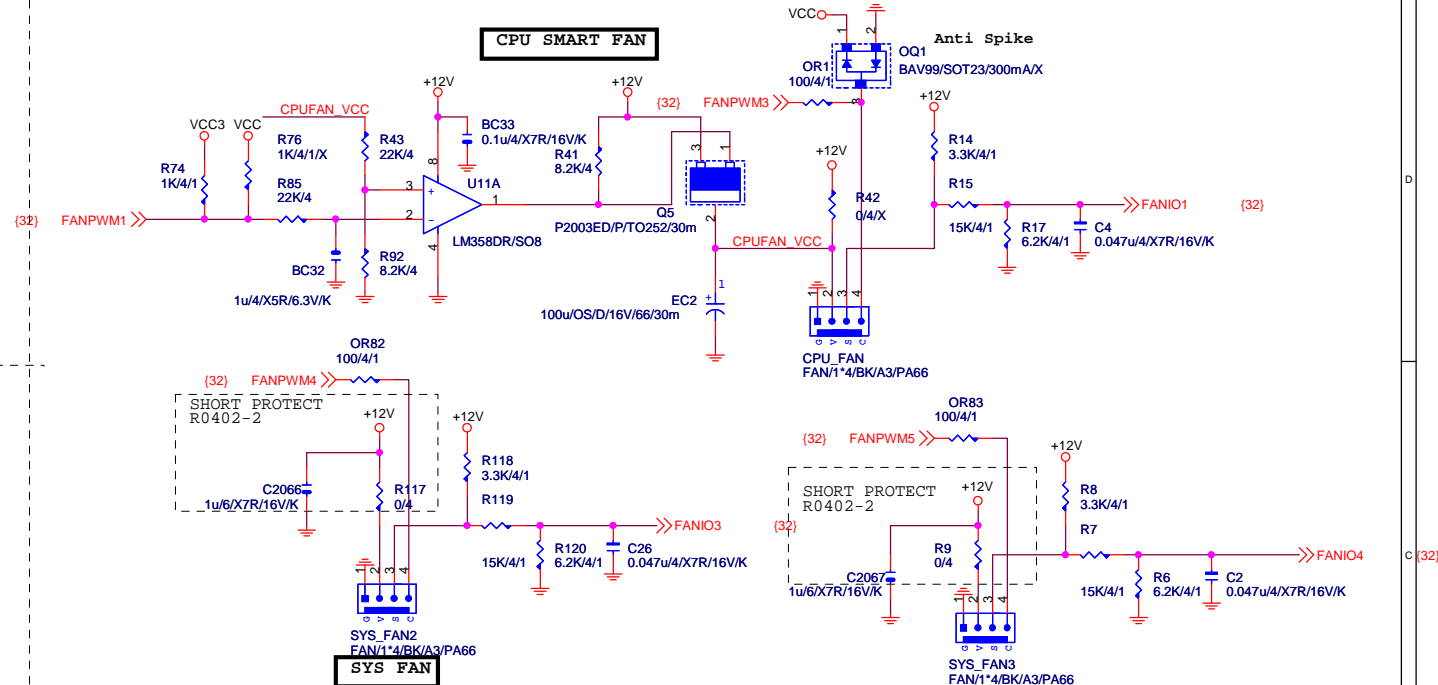
TEMP H/W MONITOR



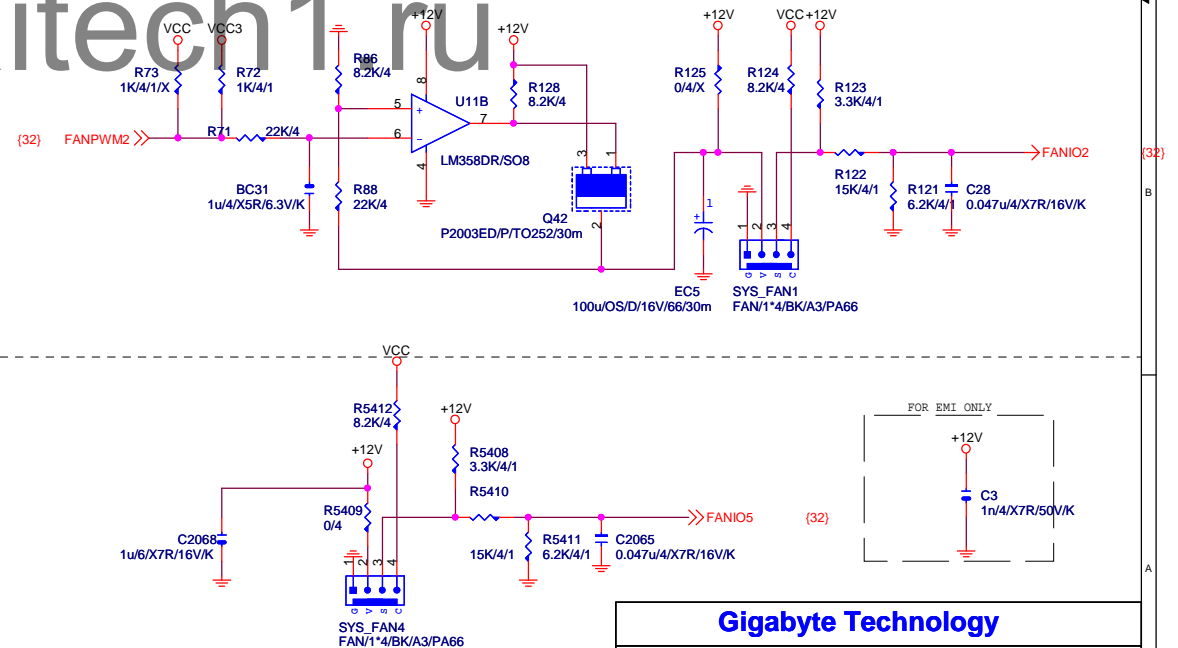
VOLTAGE-- H/W MONITOR



CPU SMART FAN



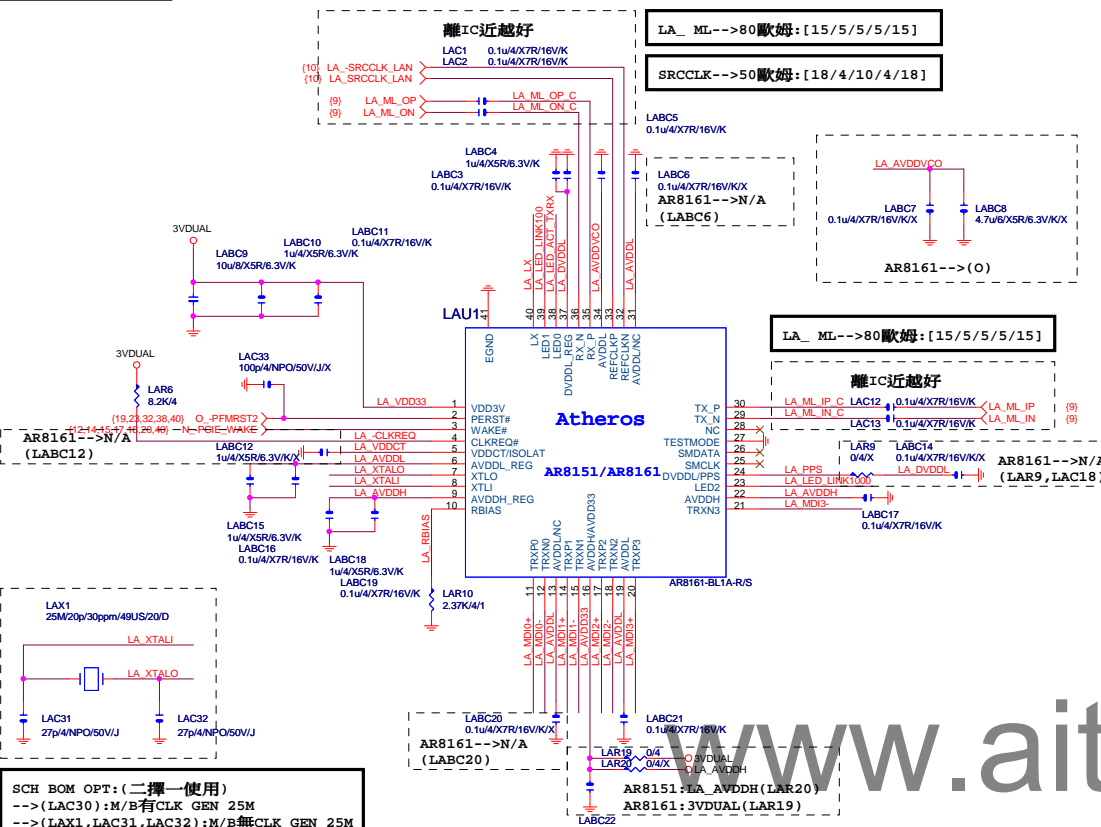
Linear SYS_FAN



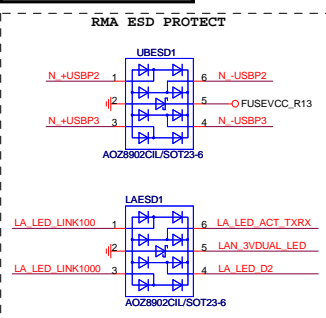
Gigabyte Technology

Title		
HWM,KB/MS, FAN CTRL		
Size	Document Number	Rev
Custom	GA-Z77X-UD3H-WB	1.1
Date:	Tuesday, August 28, 2012	Sheet 36 of 41

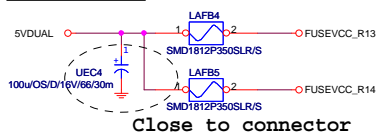
LAN:AR8151/AR8161



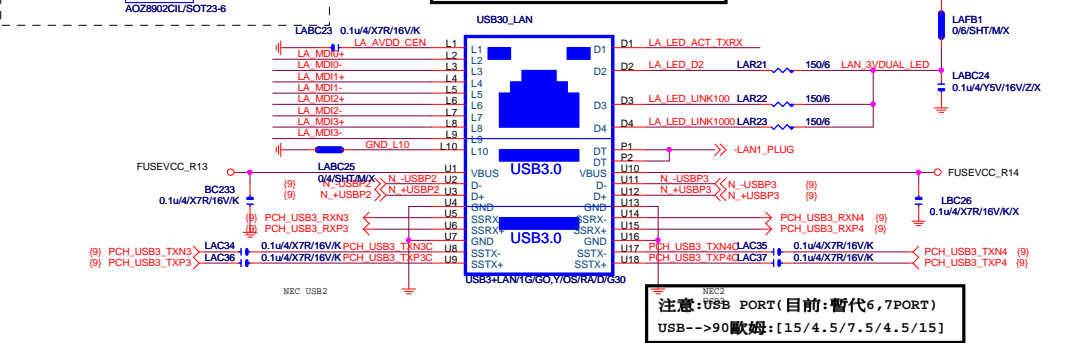
USB LAN CONNECTOR



USB X3 POWER

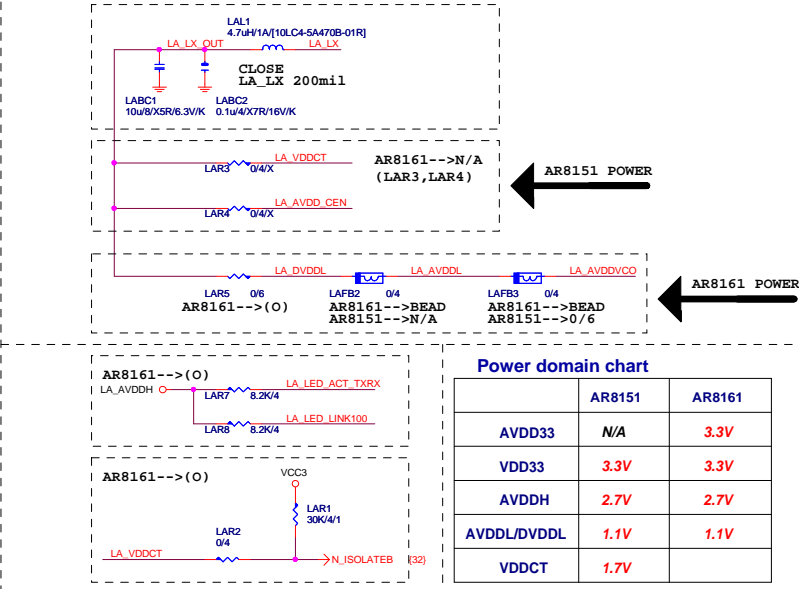


LA MPI-->100歐姆:[20/4/8/4/20]



LAN POWER

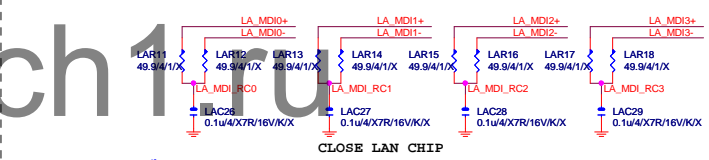
```
NEW DESIGN ONLY FOR INTERNAL SWR
AR8151:LAR3(O),LAR5(X)
AR8161:LAR5(O),LAR3/LAR4(X)
```



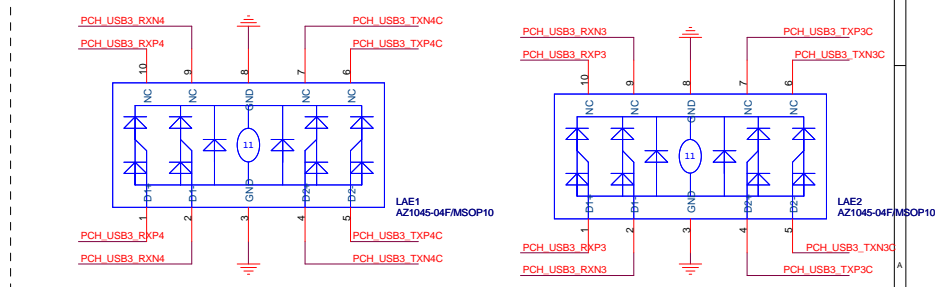
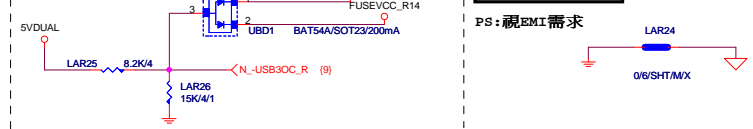
Power domain chart

	AR8151	AR8161
AVDD33	N/A	3.3V
VDD33	3.3V	3.3V
AVDDH	2.7V	2.7V
AVDDL/DVDDL	1.1V	1.1V
VDDCT	1.7V	

MDI : AR8161-->N/A

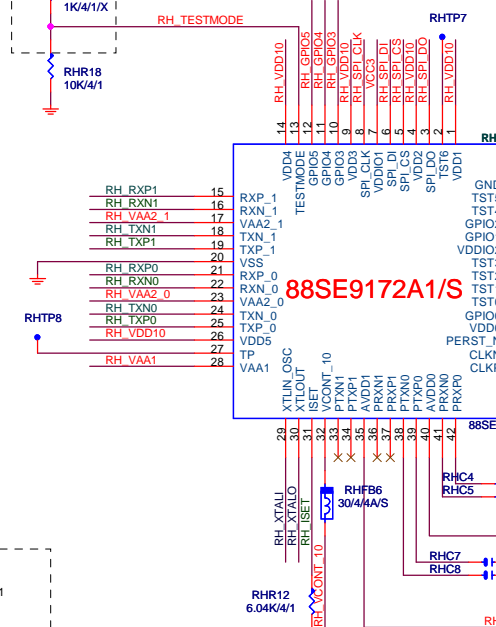
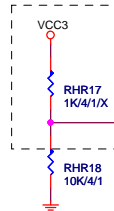
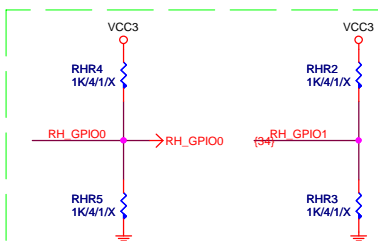
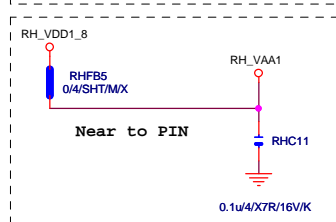
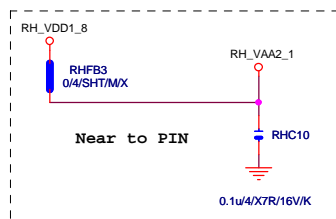
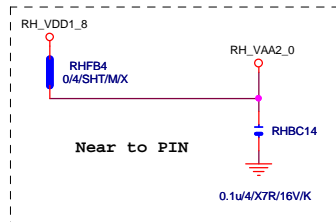
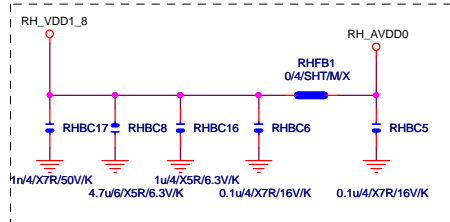
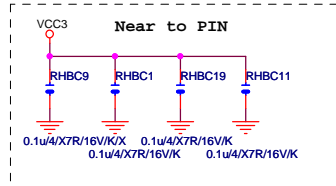
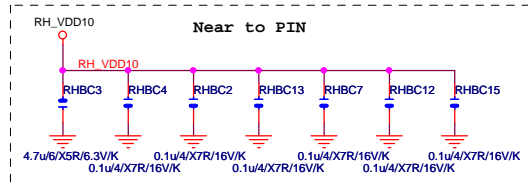


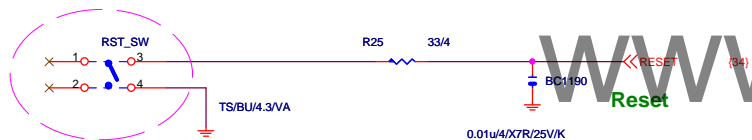
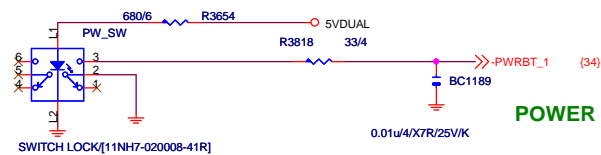
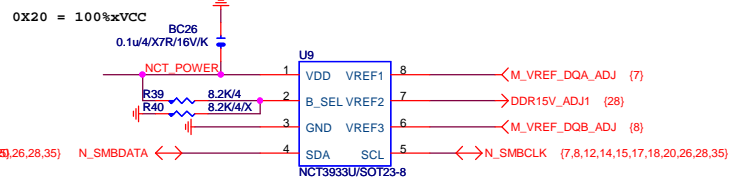
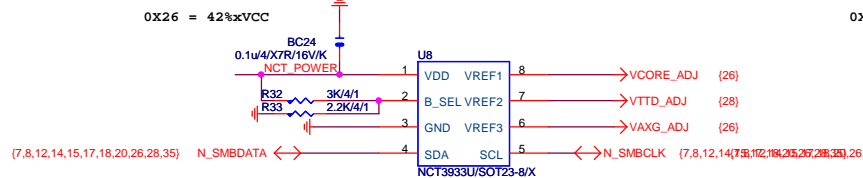
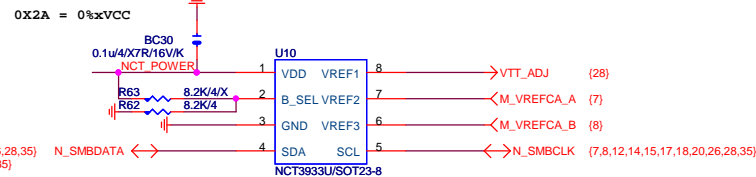
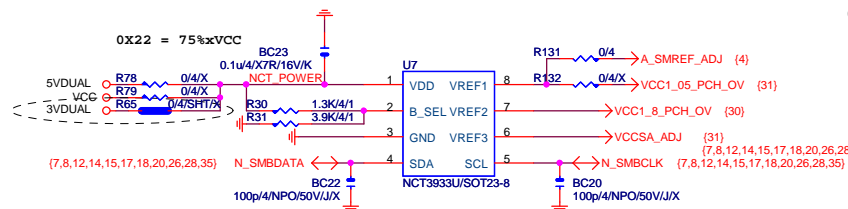
EMI SHORT PAD



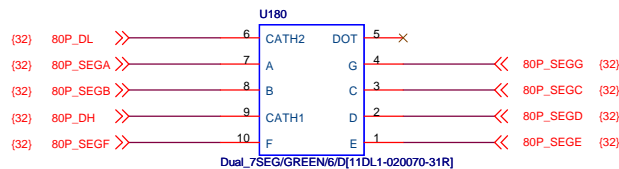
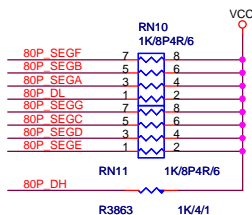
Gigabyte Technology

ARTHEROS AR8151/AR8161			
Size Custom	Document Number GA-Z77X-UD3H-WB		Rev 1.1
Date: Tuesday, August 28, 2012		Sheet 37 of 41	

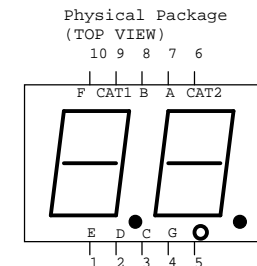


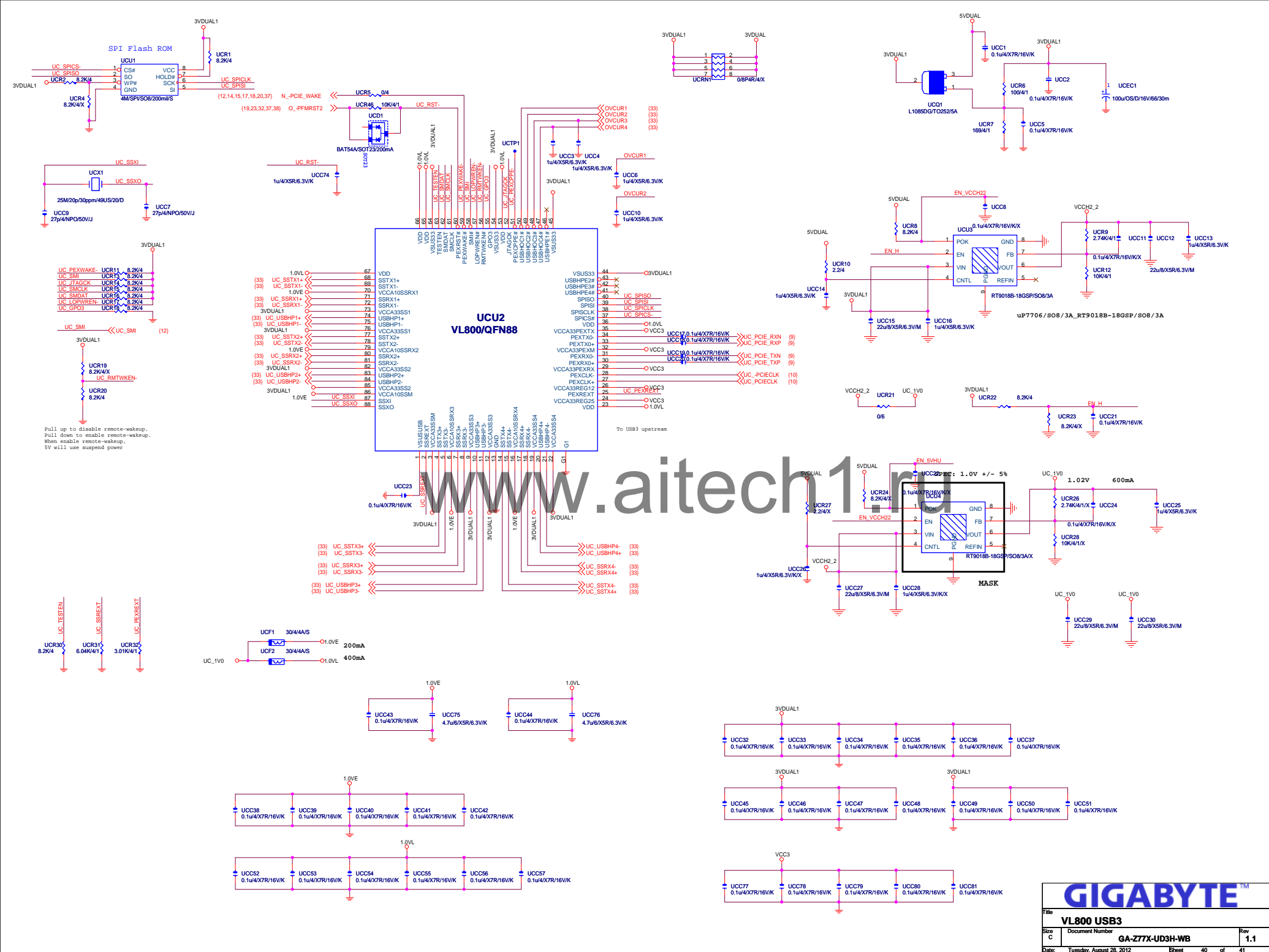


80 PORT



COMMON CATHODE



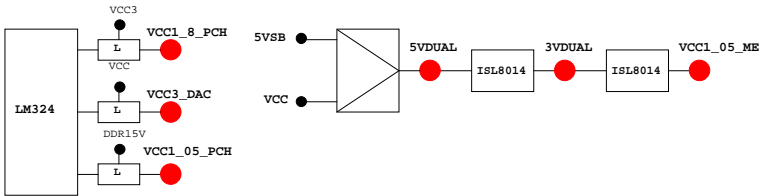


PCH GPIO LIST TABLE					
PIN NAME	PWR	Default	USAGE	NOTE	
GP0	MAIN	H-Z	GPI	-PECI_REQ	N/A
GP1/TACH1	MAIN		GPI	ICH_FAN_TACH1	N/A
GP2/PIRQE#	MAIN		GPI	-PIRQE	P/U 8.2K VCC3
GP3/PIRQF#	MAIN		GPI	-PIRQF	P/U 8.2K VCC3
GP4/PIRQG#	MAIN		GPI	-PIRQG	P/U 8.2K VCC3
GP5/PIRQH#	MAIN		GPI	-PIRQH	P/U 8.2K VCC3
GP6/TACH2	MAIN		GPI	ICH_FAN_TACH2	N/A
GP7/TACH3	MAIN		GPI	ICH_FAN_TACH3	N/A
GP8	STBY	H	GPO	GPIO8	P/U 8.2K 3VDUAL
GP9/OC5#	STBY		NATIVE	OC5#	N/A
GP10/OC6#	STBY		NATIVE	OC6#	N/A
GP11/SMBALERT#	STBY		NATIVE	-SMBALERT	P/U 8.2K 3VDUAL
GP12	STBY	L	GPI	LAN_PHY_PWR_CTRL	P/U 8.2K 3VDUAL
GP13	STBY	L	GPI	GPIO13	P/U 8.2K 3VDUAL
GP14/OC7#	STBY		NATIVE	OC7#	N/A
GP15	STBY	L	GPO	GPIO15	N/A
GP16	MAIN		GPI	-SKTOCC	P/U 8.2K VCC3
GP17/TACH0	MAIN		GPI	ICH_FAN_TACH0	N/A
GP18	MAIN		NATIVE	MB_ID0	P/D 8.2K GND
GP19	MAIN		GPI	-LAN1_ISO	P/U 8.2K VCC3
GP20	MAIN		NATIVE	LED_CTL	P/U 1K VCC3
GP21	MAIN		GPI	VCC18_PCH_OV2	P/U 8.2K VCC3
GP22	MAIN	H-Z	GPI	VCORE_OV3	P/U 8.2K VCC3
GP23	MAIN		NATIVE	-LDRQ1	P/U 8.2K VCC3
GP24	STBY	L	GPO	TLS	P/U 8.2K 3VDUAL
GP25	STBY		NATIVE	-CPU_STOP	P/U 8.2K 3VDUAL
GP26	STBY		NATIVE	-AC2_DET	P/U 8.2K 3VDUAL
GP27	STBY	H	GPO	GPIO27	P/U 8.2K 3VDUAL
GP28	STBY	H	GPO	GPIO28	P/U 8.2K 3VDUAL
GP29	STBY	L	GPI	GPIO29	N/A
GP30	STBY	H-Z	GPI	S_PWR_ACK	P/U 100K 3VDUAL
GP31	STBY	H-Z	GPI	N/A(Reverse)	P/U 8.2K VCC3
GP32	MAIN	H	GPO	MB_ID1	P/D 8.2K GND
GP33	MAIN	H	GPO	LOAD-LINE	P/U 1K VCC3
GP34	MAIN	H-Z	GPI	-PCI_STOP	P/U 8.2K VCC3
GP35	MAIN	L	GPO	GPIO35	P/U 8.2K VCC3
GP36	MAIN		GPI	-LAN1_DSM	P/U 8.2K VCC3
GP37	MAIN		GPI	N/A	P/U 8.2K VCC3
GP38	MAIN	H-Z	GPI	VCORE_OV2	P/U 8.2K VCC3
GP39	MAIN	H-Z	GPI	-LAN_DSM	P/U 8.2K VCC3
GP40	STBY		NATIVE	OC1#	N/A
GP41	STBY		NATIVE	OC2#	N/A
GP42	STBY		NATIVE	OC3#	N/A
GP43	STBY		NATIVE	OC4#	N/A
GP44	STBY	L	NATIVE	N/A	P/U 8.2K 3VDUAL
GP45	STBY		NATIVE	-LPCPME	P/U 8.2K 3VDUAL
GP46	STBY	L	NATIVE	PWR_LED	P/U 8.2K 3VDUAL
GP47	STBY		NATIVE	PSI_LED	P/U 8.2K 3VDUAL
GP48	MAIN	H-Z	IN	EN_PWM	P/U 8.2K VCC3
GP49	MAIN	H-Z	IN	VCC18_OV1	P/U 8.2K VCC3
GP50	MAIN		NATIVE	-REQ1	P/U 2.2K VCC
GP51	MAIN	H	NATIVE	-GNT1	N/A
GP52	MAIN		NATIVE	-REQ2	P/U 2.2K VCC
GP53	MAIN	H	NATIVE	-GNT2	N/A
GP54	MAIN		NATIVE	-REQ3	P/U 2.2K VCC
GP55	MAIN	H	NATIVE	-GNT3	N/A
GP56	STBY		NATIVE	N/A(Reverse)	P/U 8.2K 3VDUAL
GP57	STBY	H-Z	IN	VCORE_OV1	P/U 8.2K 3VDUAL
GP58	STBY	H-Z	NATIVE	F_USB_OC	P/U 8.2K 3VDUAL
GP59	STBY		NATIVE	USB_OC0#	N/A
GP60	STBY	H-Z	NATIVE	N/A(Reverse)	P/U 8.2K 3VDUAL
GP61	STBY	L	NATIVE	-SUSTAT	N/A
GP62	STBY	L	NATIVE	SUSCLK	N/A
GP63	STBY	L	NATIVE	GPIO63	N/A
GP64	MAIN	L	NATIVE	CLKOUTFLEX0	N/A
GP65	MAIN	L	NATIVE	CLKOUTFLEX1	N/A
GP66	MAIN	L	NATIVE	CLKOUTFLEX2	N/A
GP67	MAIN	L	NATIVE	CLKOUTFLEX3	N/A
GP72	STBY	H-Z	NATIVE	VCORE_OV4	P/U 8.2K 3VDUAL
GP73	STBY		NATIVE	1_05V_OV1	P/U 8.2K 3VDUAL
GP74	STBY	H-Z	NATIVE	1_05V_OV2	P/U 8.2K 3VDUAL
GP75	STBY	H-Z	NATIVE	N/A(Reverse)	P/U 8.2K 3VDUAL

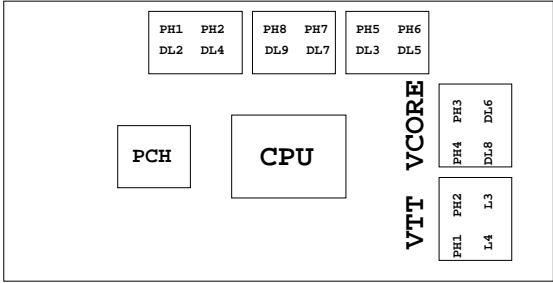
Super I/O ITE8720 GPIO Table

PIN NAME	USAGE	NOTE
SVC/PECI_RQT/GP14	-PECI_REQ	
PWROK1/GP13	PWROK1/ITE_PWROK	
KRST#/GP62	-KBRST	
SO/GP50	-ICH_SPI_CS	
IRTX/GP47/CE2_N/JP7	CEB_N	
GP46/IRRX	-LAN2_DSM	
PSION#/GP42	-PSON	
PWROK2#/GP41	PECI_CTL	
PCIRST3#/GP10/VDIMM_STR_EN	-PCIE_RST	
RSMRST#CIRRX1/GP55	-RSMRST	
PME#/GP54	-LPCPME	
PD5/GP75/BUSS00	N/A	

PIN NAME	USAGE	NOTE
FAN_TAC2/GP52	FANIO2	
FAN_TAC3/GP37	FANIO3	
VIDO3/FAN_TAC4/GP25/DSR2#	FANIO4	
FAN_CTL2/GP51	FANPWM2	
FAN_CTL3/GP36	FANPWM3	
VID4/GP34	BEEP-	
VID3/GP33	TURBO1	
VID2/GP32	TURBO0	
VCORE_GOOD/VID6/GP63	CPUT_LED1_C	
VID5/GP35	CPUT_LED2_C	
VID1/GP31	CPUT_LED3_C	
VID0/GP30	-LAN1_DSM	NBT_LED1_C
SLCT/GP80	CPU_LED1_C	
PE/GP81	CPU_LED2_C	
BUSY/GP82	CPU_LED3_C	
PD3/GP73/BUSS11	SB_LED1_C	
PD4/GP74/BUSS12	SB_LED2_C	
VCORE_EN/VID7/GP64	IT_GP64	SB_LED3_C
PD0/GP70	NB_LED1_C	
PD1/GP71	NB_LED2_C	
PD2/GP72/BUSS10	NB_LED3_C	
GP22/SEC	LOW_PWR_1	
VID05/GP27/SIN2	LOW_PWR_2	
PCIRST2#/GP11	-PFMRST1	
PCIRST1#/GP12	-PFMRST2	
3VSB5W#/GP40	CSI_F0	BSEL166_1
SUSCH#/GP53	CSI_F1	BSEL166_2
GP23/SI	BSEL166_3/CsisBSL	
VID00/GP20/CTS2#	CPUT_LED1_C	BSEL166_4
GP65/VDDA_EN/GB_01	MB_ID2	
PD6/GP76/BUSS01	MB_ID3	
PD7/GP77/BUSS02	MB_ID4	
AFD#/GP86/SMBC_R	⚡ PIN	FST_2X8
INIT#/GP85/SMBD_M	SEC_2x8	GTLREF_AD2
ACK#/GP83	DDR_LED1_C	
VID01/GP21/DCD2#	DDR_LED2_C	
STB#/GP87/SMBC_M	DDR_LED3_C	
PWRON#GP44	VCORE_OV1	
PANSWH#/GP43	PWRBTSW	
KDAT/GP61	-PWRBTSW	
KCLK/GP60	KDAT	
MDAT/GP57	KCLK	
MACL/GP56	MDAT	
GP66/VLDT_EN/GB_02	NBT_LED1_C	MCLK
SVD/PCIRSTIN#/CIRTX/GP15	PWM2_CR	
KDAT/GP61	PWM2_CR	
GP67/CPU_PG/GB_03	EN_LOADLINE	IT_GP67/-EN_PWM2
SLIN#/GP84/SMBD_R	-EN_PWM2	
PSI_L/FAN_CLT15/CIRRX2/GP16	-THERM	
VIDO4/GP26/SOUT2	DDR18V_PH2_EN	
VIDO2/FAN_TAC5/GP24/DSR2#	DDR18V_LED	
VIDO6/GP17/RI2#	1_1V_PH_EN	
VIDO7/JP6/DTR2#	JP6	
PD5/GP75/BUSS00	SB_LED3_C	



PWM各相位的擺法如下：



BIOS超電壓對應表：

線路圖名稱	BIOS選項
Vcore	CPU Vcore
CPU_VTT	CPU Termination
CPU_VAXG	CPU Graphic Core
VCC1_8_PCH	CPU PLL
VCC1_05_PCH	PCH core
3VDUAL	3VDUAL
DDR15V	DRAM voltage
DDRVTT	DRAM Terminatio
VREF_CA_AVREF_CA_B	DRAM Address Ref
VREF_DQ_AVREF_DQ_B	DRAM Data Ref

散熱模組料號：

8IBP：
1.12SP2-01A001-Y1R/Y2R
2.12SP2-01A001-Z1R/Z2R
(HIBRID模組)包材階

	3 pin FAN control	4 pin FAN control	FAN speed	Controller
CPU FAN	FANPWM1	FANPWM3	FANIO1	IT8720
	ICH_FAN_PWM2	ICH_FAN_PWM0	ICH_FAN_TACH0	PCH
SYS FAN	FANPWM2	N/A	FANIO2	IT8720
	ICH_FAN_PWM1	N/A	ICH_FAN_TACH1	PCH
PWR FAN	N/A	N/A	FANIO3	IT8720
			ICH_FAN_TACH2	PCH

Gigabyte Technology			
TABLE LIST			
Size C	Document Number	Rev	
	GA-Z77X-UD3H-WB	1.1	
Date:	Tuesday, August 28, 2012	Sheet	41 of 41